## DESCRIPTION

The SCT61240 is a highly integrated power management IC (PMIC) optimized for camera system. It integrates three high efficiency synchronous BUCK converters (HVBUCK1, LVBUCK2, LVBUCK3), and a high-

## APPLICATIONS

- ADAS
- Compact Camera Module
- Cabin Monitor

PIN FUNCTIONS (continued)

| NAME | NO. | DESCRIPTION |
|---|---|---|
| AGND | 5 | Analog ground. AGND is the reference GND for the internal logic and signal circuit. AGND is not internally connected to Power Ground, make sure AGND connected to power ground in PCB. |
| [redacted] | [redacted] | [redacted]ect a 2.2 or larger decouple ceramic |
| LDOOUT | 7 | ceramic decouple capacitor between this pin and ground. |

NR

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## ELECTRICAL CHARACTERISTICS

$V_{IN}$=10V, $T_A$=-40°C~150°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power Supply | | | | | | |
| $V_{IN}$ | Operating input voltage | | 4 | | 19 | V |
| $V_{IN_UVLO}$ | Input UVLO Rising Threshold | | 3.6 | 3.8 | 3.95 | V |
| | Hysteresis | | | 200 | | mV |
| $I_{SHDN}$ | Shutdown current from VIN pin | EN=0, no load | | 1 | 10 | A |
| $I_Q$ | Quiescent current from VIN pin | EN=3V, no load, non-switching | | 1 | 2 | mA |
| $I_{Q_ACTIVE}$(1) | Quiescent current from VIN pin | EN=3V, no load, switching | | 10 | | mA |
| Enable | | | | | | |
| $V_{EN}$ | EN rising threshold | | 1.1 | 1.2 | 1.3 | V |
| | EN hysteresis | | | 100 | | mV |
| $I_{EN}$ | EN Pin Input Leakage | EN=5V, VIN=0V | | 0.01 | 1 | A |
| Oscillator and Timing | | | | | | |
| $F_{SW}$ | Switching Frequency | | 2 | 2.2 | 2.4 | MHz |
| FSS | Spread Spectrum range | | 4 | 5 | 6 | % |
| | Spread Spectrum frequency | | 3.5 | 4.3 | 5 | kHz |
| $T_{ON_MIN}$ | Minimum On Time | | | 60 | | ns |
| $T_{OFF_MIN}$ | Minimum Off Time | | | 60 | | ns |
| $T_{SS_BK1}$ | BUCK1 soft start time | $V_{OUT1}$=3.1V, from 0 to 100% | | 400 | | s |
| $T_{SS_BK2}$ | BUCK2 soft start time | $V_{OUT2}$=1.8V, from 0 to 100% | | 400 | | s |
| $T_{SS_BK3}$ | BUCK3 soft start time | $V_{OUT3}$=1.2V, from 0 to 100% | | 400 | | s |
| $T_{SS_LDO}$ | LDO soft start time | $V_{OUT4}$=2.8V, $C_{NR}$=100nF, $C_{OUT}$=10 F, $I_{LOAD}$=100mA | | 100 | 300 | s |
| $T_{PG_delay}$(1) | PG delay | Default setting | | 3.6 | | ms |
| $T_{hiccup}$ | Hiccup time | | 2 | 3.6 | 5.2 | ms |
| BUCK1 (HV BUCK) | | | | | | |
| $V_{OUT1}$ | VOUT1 Output Voltage | SCT61240 | | 3.3 | | V |
| | | SCT61240-0000 | | $V_{LDO}$+0.3 | | |
| | | SCT61240-0001 | | $V_{LDO}$+0.5 | | |
| $V_{OUT1_ACC}$ | | | | | | |

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## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$=10V, $T_A$=-40°C~150°C, typical values are tested under 25°C

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DIS_BUCK1}$ | VOUT1 Output Discharge resistance | | 30 | 50 | 70 | Ohm |
| BUCK2 (LV BUCK) | | | | | | |
| $V_{IN23}$ | VIN23 Input Voltage Range | | 2.7 | | 5 | V |
| $V_{OUT2}$ | VOUT2 Output Voltage | | | 1.8 | | V |
| $V_{OUT2_ACC}$ | VOUT2 Accuracy | | -2 | | 2 | % |
| $R_{DS_H_BK2}$ | High-side MOSFET on-resistance | $V_{OUT1}$=3.1V | | 155 | 260 | m |
| $R_{DS_L_BK2}$ | Low-side MOSFET on-resistance | VIN>5V | | 75 | 125 | m |
| $I_{ILEAK_HS_BUCK2}$ | SW2 HS Switch Leakage Current | $T_A$=25°C | | 0.01 | 1 | A |
| | | $T_A$=-40°C~150°C | | 7 | | A |
| $I_{ILEAK_LS_BUCK2}$ | SW2 LS Switch Leakage Current | | | 0.01 | 1 | A |
| $I_{PEAK_BUCK2}$ | Peak Current Limit | | 0.9 | 1.2 | 1.65 | A |
| $I_{VALLEY_BUCK2}$ | Valley Current Limit | | 0.65 | 1 | 1.3 | A |
| $I_{REVERSE_BUCK2}$ | Reverse Current Limit | | 0.4 | 0.7 | 1 | A |
| $I_{ILEAK_VOUT2}$ | VOUT2 PIN Leakage | | | 1 | 10 | A |
| $R_{DIS_BUCK2}$ | VOUT2 Output Discharge resistance | | 30 | 50 | 70 | Ohm |
| BUCK3 (LV BUCK) | | | | | | |
| $V_{IN23}$ | rD17Q ent /P < Tw 1.107 04.61 | | | | | |

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## ELECTRICAL CHARACTERISTICS (Continued)

$V_{IN}$=10V, $T_A$=-40°C~150°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DROP_LDO}$ | LDO Dropout Voltage | LDOIN=2.9V, setting LDO output =2.8V, ILDO = 300mA | | 110 | 200 | mV |
| $L_{DO_LINE_REG}$ | LDO Line Regulation | LDOOUT set to 2..16 Tm 531..48 | | | | |

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## TYPICAL CHARACTERISTICS

$V_{IN}$=10V, $T_A$=-40°C~125°C, unless otherwise noted.



Figure 1. Buck1 Efficiency vs Load Current, $V_{OUT1}$=3.2V

Figure 2. Buck1 Efficiency vs Load Current, $V_{OUT1}$=3.0V

Figure 3. Buck2 Efficiency vs. Load Current, $V_{OUT2}$=1.8V

Figure 4. Buck3 Efficiency vs. Load Current, $V_{OUT3}$=1.2V

Figure 5. Buck3 Efficiency vs. Load Current, $V_{OUT3}$=1.5V

Figure 6. Buck1 Peak Current Limit vs. Temperature

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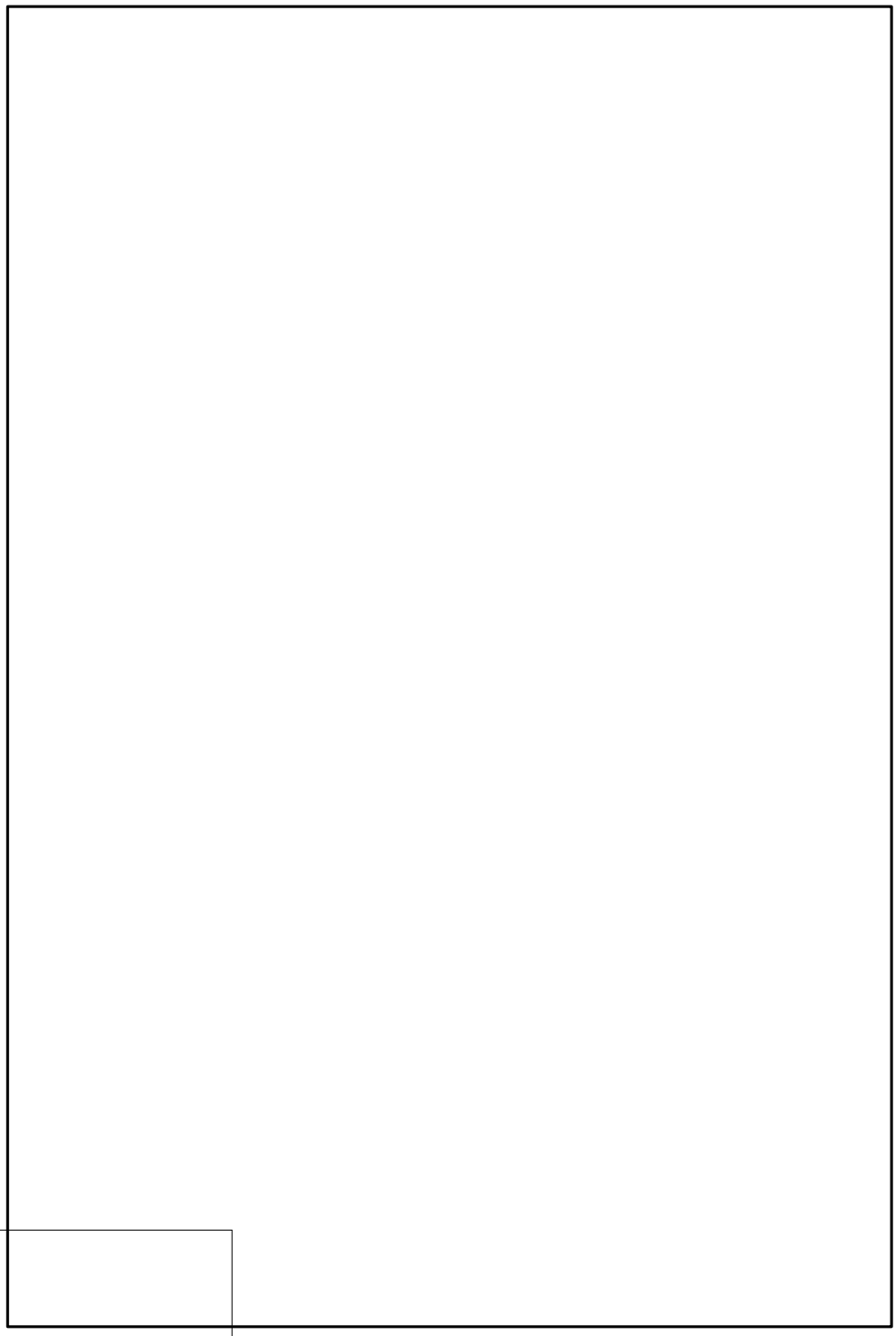
## FUNCTIONAL BLOCK DIAGRAM



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# OPERATION

## Overview

The SCT61240 is a highly integrated power management IC (PMIC) optimized for camera system. It integrates three high efficiency synchronous BUCK converters (HVBUCK1, LVBUCK2, LVBUCK3), and a high-PSRR low noise LDO with OV/UV monitoring on all outputs.

VOUT1 is the output of BUCK1, which is powered from VIN (Power Over Coax) and can output 1.2A continuous current with the output voltage set to LDOOUT+300mV/500mV or fixed 3.3V.

VOUT2 is the output of BUCK2, which is powered from VOUT1 and can output 600mA continuous current with the output voltage fixed to 1.8V.

VOUT3 is the output of BUCK3, which is powered from VOUT1 and can output 1.2A continuous current with the output voltage set to 1.1V/1.2V/1.3V/1.5V through RSET PIN for different sensors.

LDOOUT is the output of LDO, which is powered from VOUT1 (need to connect LDOIN to VOUT1) and can output 300mA continuous current with the output voltage set to 2.7V/2.8V/2.9V/3.3V through RSET PIN for different sensors.

With a compact QFN2.5x3.5 package, the SCT61240 greatly reduces external components count and PCB space.

## VIN and EN UVLO

When the VIN pin voltage rises above 3.8V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 3.8V or when the EN pin voltage is below 1.1V.

An internal 10M r pulls EN pin to an internal 5V power supply allows the device to be enabled when EN pin is floating to simplify the system design.

## High Efficiency Buck Converters

All the 3 BUCKs employ 2.2MHz fixed frequency peak current mode control with forced continuous conduction mode (FCCM). Built-in UVLO, soft-start (0.5ms/1ms/1.5ms/2ms options by OTP trim), compensation and hiccup (or

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Under Voltage Protection

If an output falls below the under voltage protection threshold, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting. When entry hiccup, the output discharge will operate during the hiccup time.

Over Current Protection (OCP)

For the three bucks and LDO, the SCT61240 provides both peak and valley current limit designed to limit the peak/valley inductor current to ensure that the switching currents remain within the device capabilities during overload conditions or during an output short circuit.

When the HS-FET turns on, the chip monitors the increased IL through the relevant operating main power switch. Once the peak IL exceeds the peak current limit threshold, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease IL. The HS-FET does not turn on again until IL falls below the valley current limit threshold. If the feedback voltage makes EA's output level triggers the high clamp limit consecutively in a settled cycle, an over-current (OC) fault is reported and OCP is activated, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting.

Power Good

The PG pin is a push-pull output. It goes to logic high when the device is powered on, and all outputs are within the power good range, and no faults reported. The high output level can be programmed to either 3.3V or 1.8V.

PG will assert low when any of below events occur:

- Buck1's output is out of power good range or VOUT OV/UV range or OCP
- Buck2's output is out of power good range or VOUT OV/UV range or OCP
- Buck3's output is out of power good range or VOUT OV/UV range or OCP
- LDO's output is out of power good range or VOUT OV/UV range or OCP
- Junction temperature is over Thermal Shutdown point
- VIN is higher than VIN OVP threshold

Hiccup or L atch off P rotection

When below faults are detected, the SCT61240 will enter hiccup or latch off mode (programmable option). When select hiccup mode and entry hiccup, all the channels shut off for 3.2ms, and then the normal power up sequence will start again according to the SEQ and RSET setting. When select latch off mode and entry latch off, all the channels shut off and not restart unless VIN/EN power on reset (POR).

The faults that make the device entry hiccup/latch off protection:

- Buck1's output is out of VOUT OV/UV range or OCP
- Buck2's output is out of VOUT OV/UV range or OCP
- Buck3's output is out of VOUT OV/UV range or OCP
- LDO's output is out of VOUT OV/UV range or OCP
- Junction temperature is over Thermal Shutdown point
-

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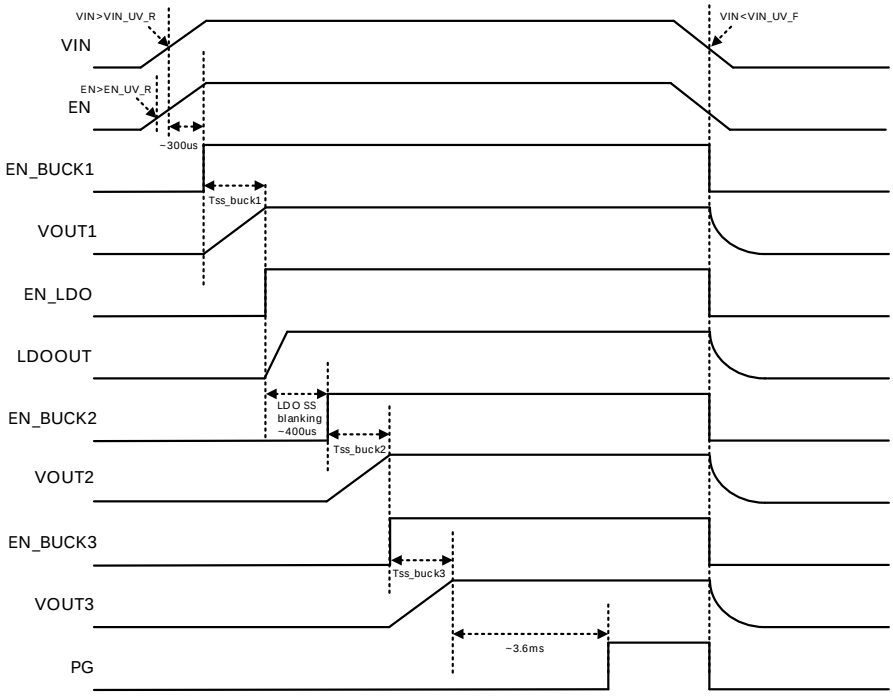


Figure 12. Example SEQ1 for SCT61240

Output Voltage Setting

The device provides 9 flexible voltage setting through RSET PIN for various sensors. Connect a resistor between RSET and GND to set the output voltage of each channel before enabling the device. The RSET detection only activated at the beginning of power on, and the output voltage configuration is latched once RSET detection done. Any change during the power on procedure is not guarantee to the correct output voltage setting.

Below table shows the output voltage setting with its corresponding resistance.

Table 2. Output Voltage Setting

| RSET No. | RSET Resistance( |
|---|---|

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# APPLICATION INFORMATION

## Typical Application

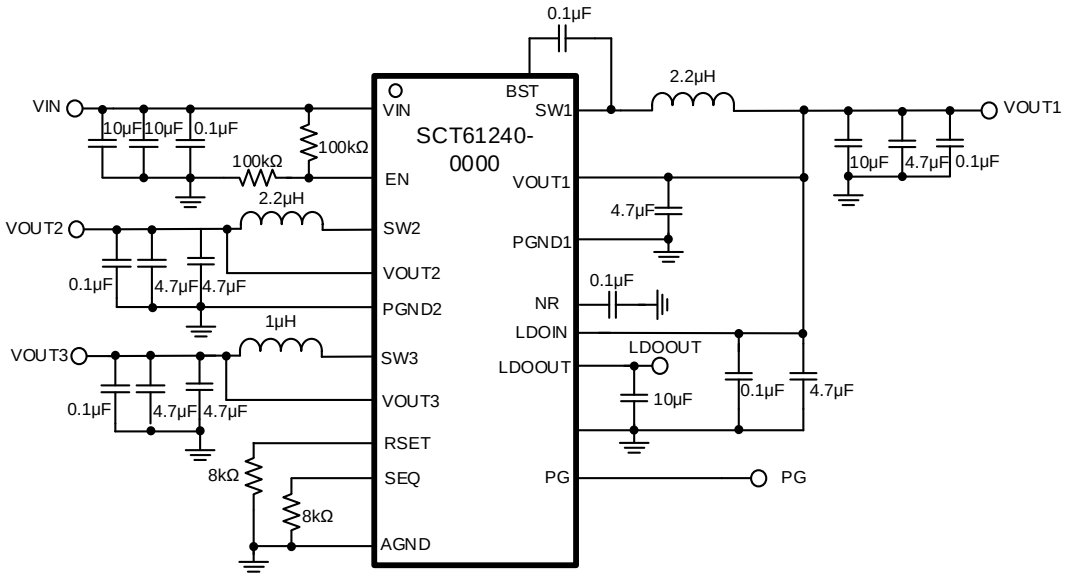


Figure 13. Application Schematic, 4V to 19V, PMIC Regulator at 2.2MHz

Design Parameters

| Design Parameters | Example Value |
|---|---|
| Input Voltage | 10V Normal 4V to 19V |
| Output Voltage | VOUT1: 3<br>LDOOUT: 2.7V |
| Maximum Output Current | VOUT1: 1.2A<br>LDOOUT: 0.3A |
| Switching Frequenc y | 2.2MHz |
| Output Voltage Ripple (peak to peak) | VOUT1: 1<br>VOUT3: 4m |

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Under Voltage Lock-Out

An external voltage divider network of $R_1$ from the input to EN pin and $R_2$ from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of $R_1$ and $R_2$ resistors.

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- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of $I_{LPP}$

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Application Waveforms

Vin=10V, RSET=SEQ=8kΩ, $V_{OUT1}$=3.0V, $V_{OUT2}$=1.8V, $V_{OUT3}$=1.2V, $V_{OUT4}$=2.7V,unless otherwise noted

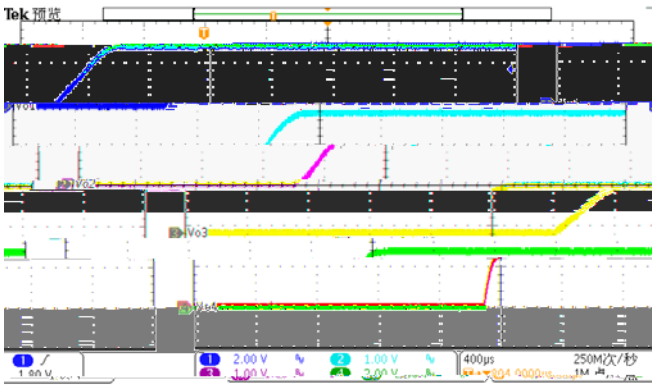

Figure 15. Power On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

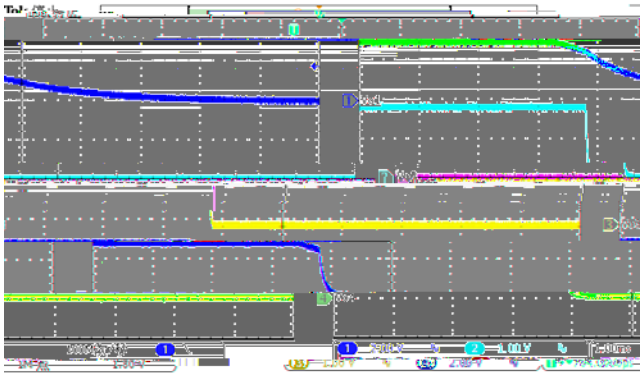

Figure 16. Power Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

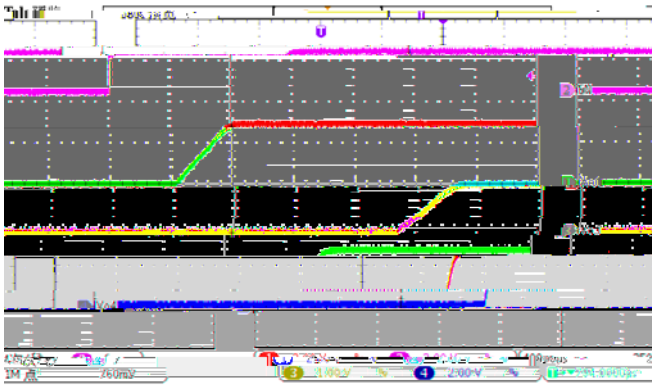

Figure 17. EN On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

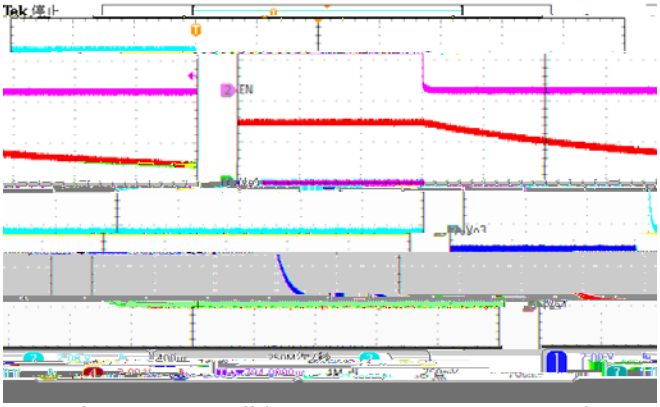

Figure 18. EN Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

Figure 19. Buck1 Over Current Protection

(1.2A to hard short)

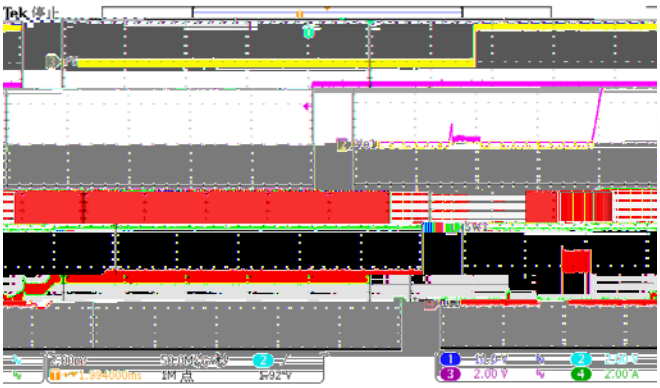

Figure 20. Buck1 Over Current Release

(hard short to 1.2A)

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Application Waveforms (continued)

Vin=10V, RSET=SEQ=8kΩ, $V_{OUT1}$=3.0V, $V_{OUT2}$=1.8V, $V_{OUT3}$=1.2V, $V_{OUT4}$=2.7V,unless otherwise noted

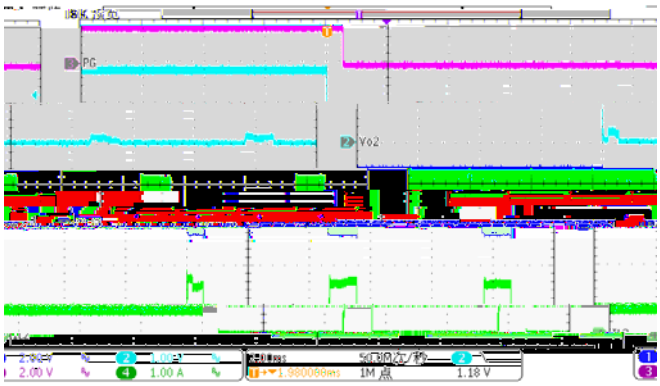


Figure 21. Buck2 Over Current Protection

(0.6A to hard short)

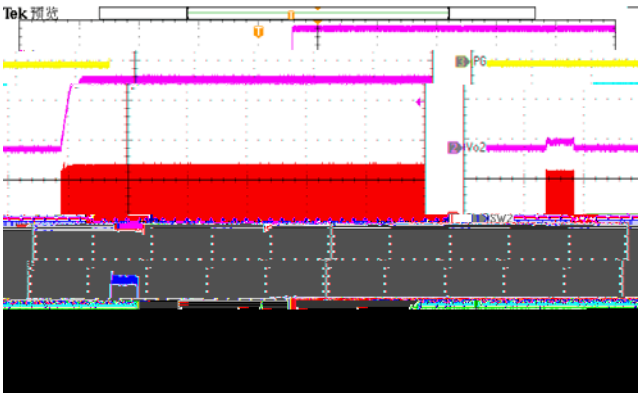


Figure 22. Buck2 Over Current Release

(hard short to 0.6A)

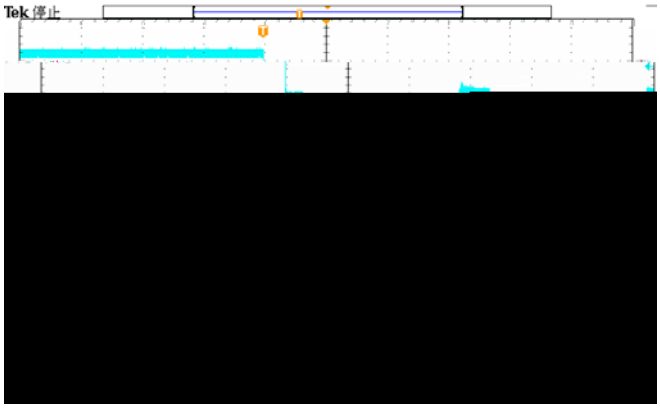


Figure 23. Buck3 Over Current Protection

(1.2A to hard short)

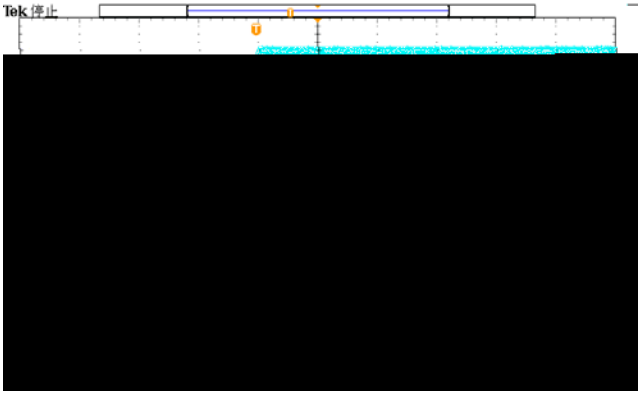


Figure 24. Buck3 Over Current Release

(hard short to 1.2A)

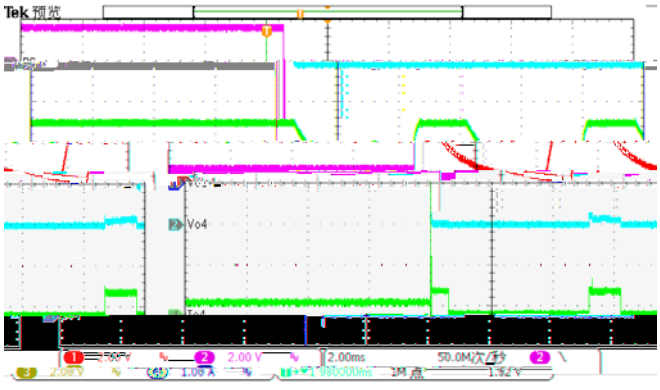


Figure 25. LDO Over Current Protection

(0.3A to hard short)

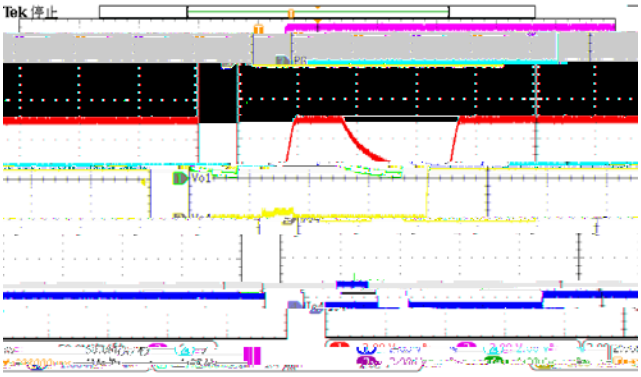


Figure 26. LDO Over Current Release

(hard short to 0.3A)

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Layout Guideline

Proper PCB layout is a critical for SCT61240's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The .2 ( 2u4 (m)-24.b(ed)]TJ 0 Tc 0 Tw ( )Tj -0.002 Tc 0.11 3 -1.112 0 Td3 (of)-13.2 ( )0.1 (r)-

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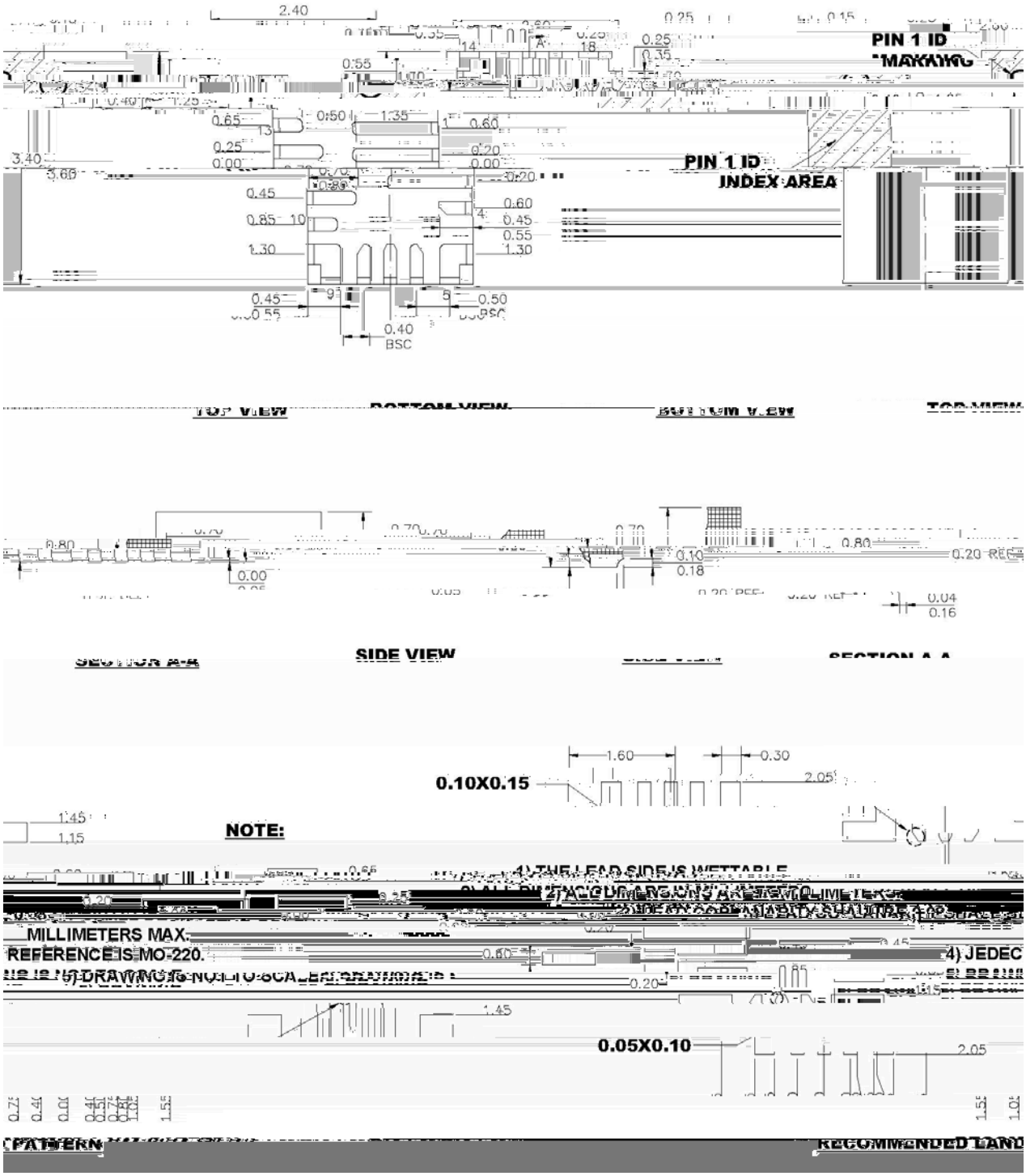
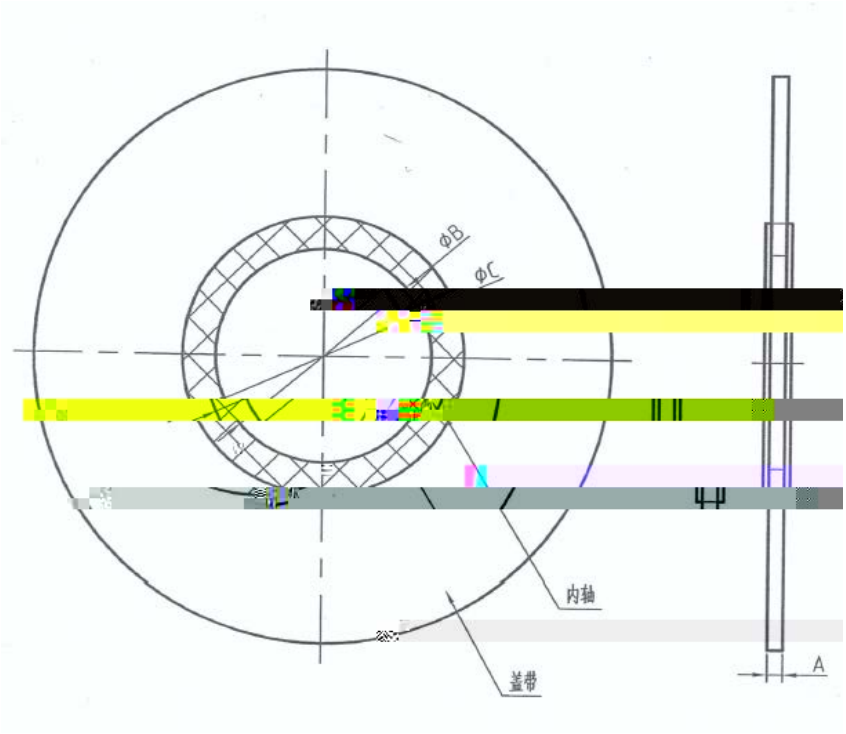
## PACKAGE INFORMATION



## TAPE AND REEL INFORMATION




| Type | $A_0^{+0.1}$ mm | Carrier Width | Diameter |
|---|---|---|---|
| PRA F4DK | 9.3 | 12 | B=76.2±0.10mm<br>C=92.2±0.25mm |
| HST | 9.5 | 12 | |
| HST | 13.5 | 16 | |
| HST C800 | 21.3 | 24 | |
| 2420S | 13.3 | 16 | |
| 2420S | 21.3 | 24 | |
| TIST300 | 9.9 | 12 | |

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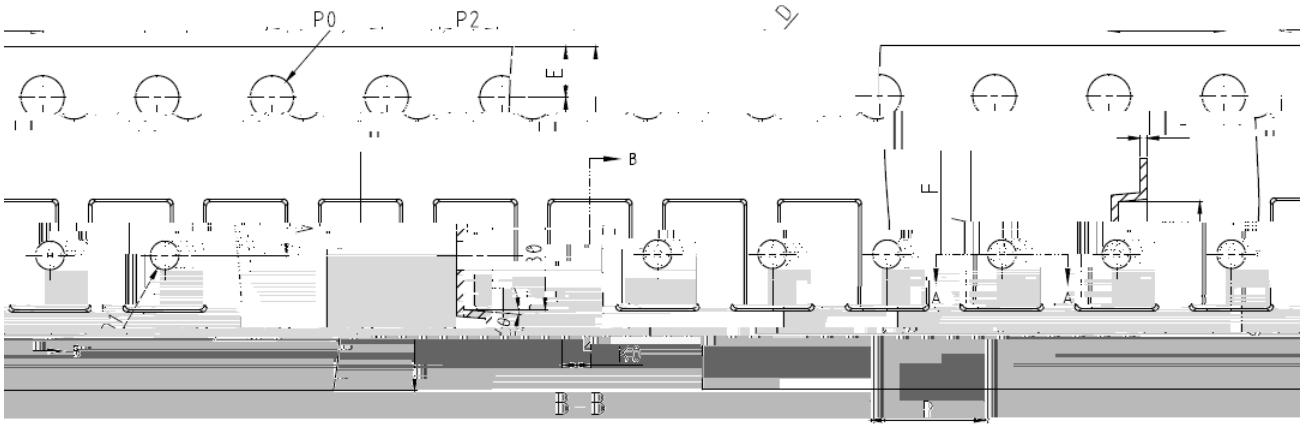


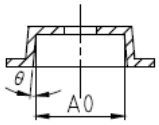


A – A

| Symbol | Dimensions in Millimeters |
|---|---|
| A0 | 2.75±0.10 |
| B0 | 3.75±0.10 |
| D | $1.5^{+0.10}$ |
| D1 | 1.00±0.10 |
| E | 1.75±0.10 |
| F | 5.50±0.05 |
| K0 | 1.00±0.10 |
| P | 4.00±0.10 |
| P0 | 4.00±0.10 |
| P2 | 2.00±0.05 |
| t | 0.25±0.03 |
| W | $12.00^{+0.30}_{-0.10}$ |
| | 5° max |

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