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M M

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update T_J to 150 ºC

Revision 1.2: Update DEVICE ORDER INFORMATION

P M M N M

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT1270FQAR	Tape & Reel	3000	1270	11	11-

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P PN N N NP P M

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN

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PN NP N NP P M

Figure 1. SCT1270 Efficiency vs Load Current, Vout=9V

Figure 2. SCT1270 Efficiency vs Load Current, Vin=3.6V

Figure 3. Load Regulation (Vin=3.6V, Vout=9V)

Figure 4. Line Regulation, Vout=9V

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Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 3. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

4¿ Ë ¾ Ê 1 x Û: 5 ÙÄ È F 6½ ¾ Å º Ù Ûï À Æ Å Ï º ¿

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calculations and bench evaluation. In this application, the

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$$\% \; L \frac{' 5 \; 4 \; H \; \%}{4_9} \qquad (18)$$

If the calculated value of C6 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

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Application Waveforms(continued)

Vin=3.6V, Vout=9V, unless otherwise noted

Figure 15. Load transient (0.2A-1.8A, 1.6A/us)

Figure 16. Load transient

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Layout Guideline

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Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

$$2_{½:Æ°Ñ} L \frac{s\ w\ I F\ 6\ \%}{4_{\sim NE}} \quad (19)$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT1270 QFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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TOP VIEW

BOTTOM VIEW

SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220

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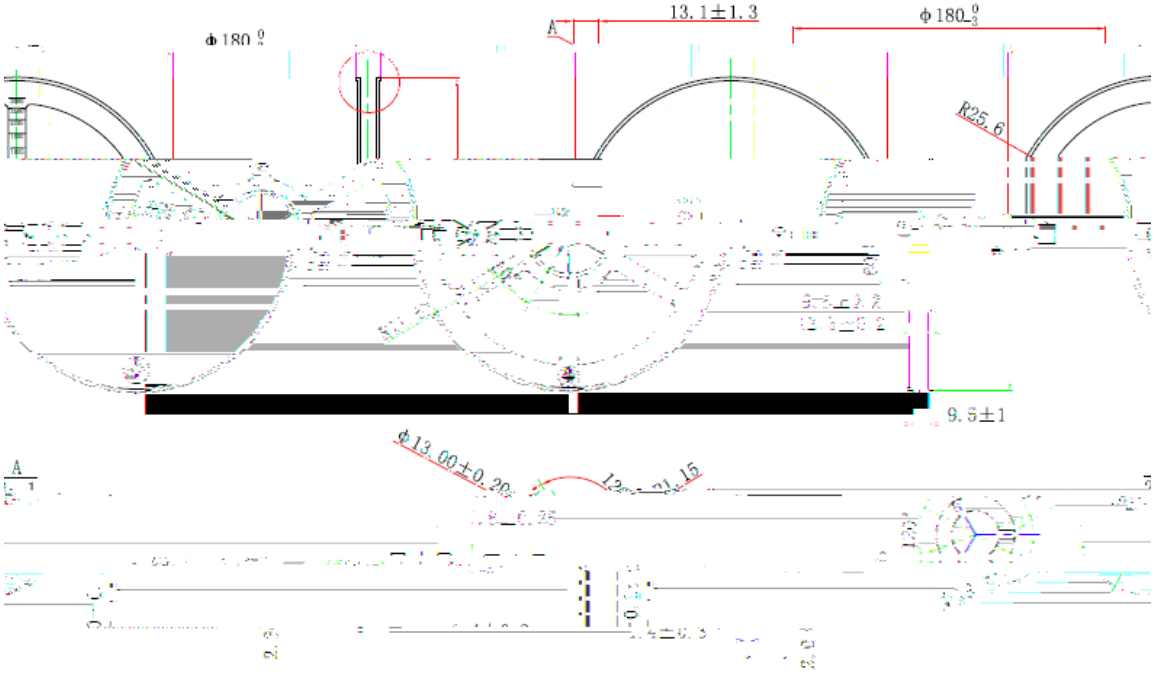
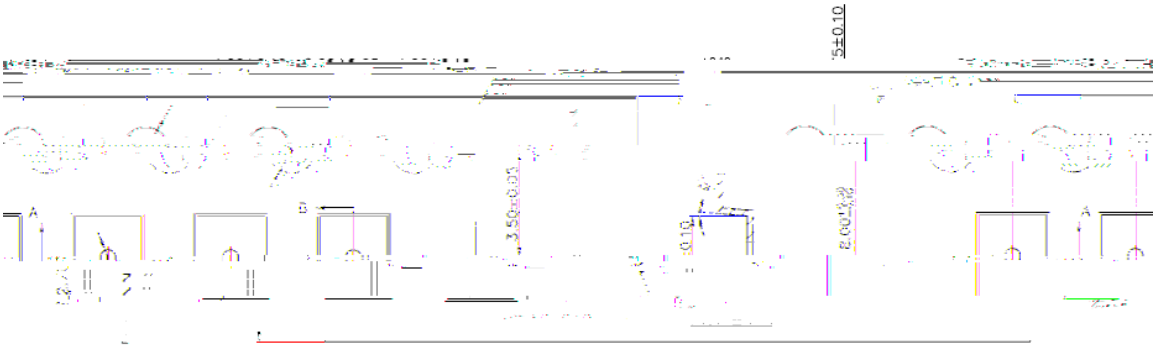
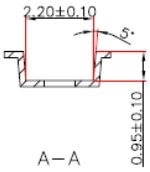




B–B



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