FSEL	4	Switching frequency selection. Connecting to ground sets clock frequency to 400KHz. Floating sets clock frequency to 800KHz. Connecting to VCC sets clock frequency to 1.2MHz.
VOUT	5	VOUT is used to sense the output voltage of the buck regulator. Connect VOUT to the output capacitor of the regulator directly. Keep the VOUT sensing trace far away from the SW node. VIAs should also be avoided on the VOUT sensing trace. A trace larger than 25mil is required.
MODE	6	PFM, USM or FCCM mode selection. Connect the pin to VCC to force the device in Forced Continuous Current Modulation (FCCM) operation mode. Ground the pin to operate the device in Pulse Frequency Modulation (PFM) mode without Ultrasonic Mode (USM). Floating the pin to operate the device in PFM with USM.
SW	7	Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time. Use wide and short PCB traces to make the connection. Keep the SW pattern area minimized.
BST	8	Bootstrap. Must connect a 0.1uF capacitor or greater between SW and BST to form a floating supply across the gate driver of high-side power MOSFET.
VCC	9	Internal VCC LDO output. The driver and control circuits are powered by VCC. Decouple with 1μF ceramic capacitor placed as close to VCC as possible.
AGND	10	Signal logic ground. AGND is the Kelvin connection to PGND.
FB	11	Feedback voltage Input. Connect FB to the tap of a resistor divider from output voltage to AGND to set up output voltage. The device regulates FB to the internal reference value of 0.6V typical.
EN	12	Enable logic input. EN is a digital input that controls the converter on or off. EN high turns on the device and EN low turns off the device. Connecting to VIN with a 100kΩ pull-up resistor can enable the device. Floating EN pin automatically starts up the converter.

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	4.5	18	V
V_{OUT}	Output voltage range	0.6	7	V
T_J	Operating junction temperature	-40	125	°C

V_{ESD}	Human Body Model (HBM), per			

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(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2260A is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2260A. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

V_{IN}=12V, T_J=-40°C~125

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PG_{TD}	PG low to high delay			0.5		ms
V_{PG}	Power Good PG pull-down strength	I_{PG} =4mA		0.6		V
I_{PG_LEAK}	Power Good PG leakage current	V_{PG}=5V			5	uA

I_{LIM_P}	LS MOSFET positive current limit	From source to drain	7.5	8.5	9.5	A
I_{LIM_N}	LS MOSFET negative current limit	From drain to source, MODE connects to VCC		2.5		A
T_{HICCUP}	Hiccup waiting time			7		ms
V_{OVP_R}	V_{FB} OVP threshold % of V_{REF}	V_{FB} rising		122		%
V_{OVP_F}	V_{FB} OVP threshold % of V_{REF}	V_{FB} falling		117		%
V_{UVP_F}	V_{FB} UVP threshold % of V_{REF}					

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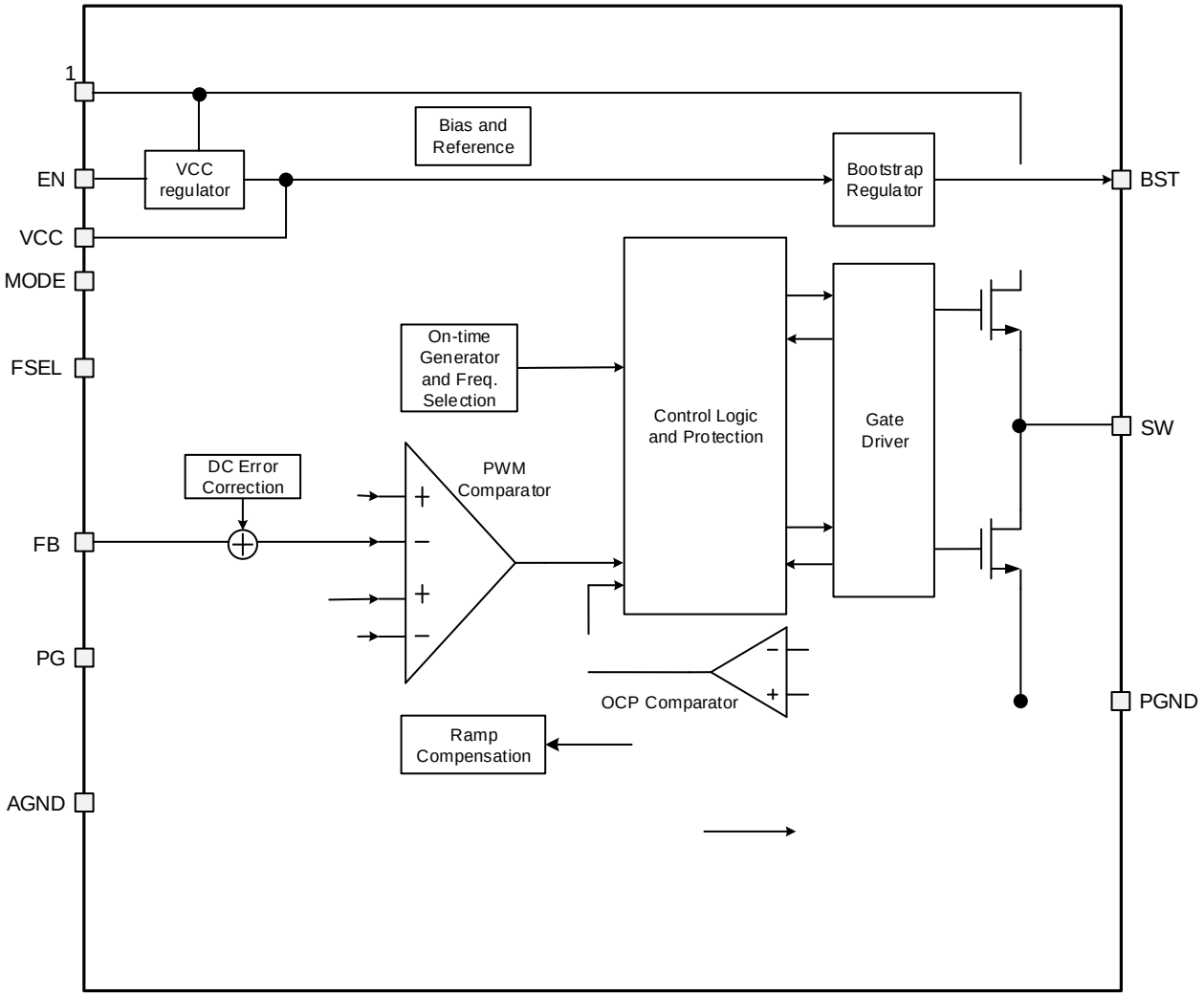

Figure 8. Functional Block Diagram

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efficiency in light load is much lower than heavy load.

The SCT2260A is enabled when the VIN pin voltage rises above 4.25V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 3.98V or when the EN pin voltage is below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

— (1)

— (2)

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

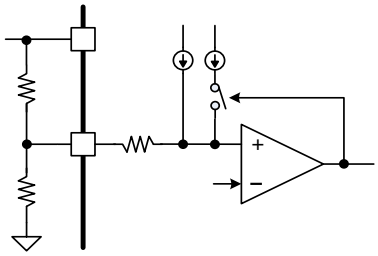

Figure 9. System UVLO by enable divide

The SCT2260A regulates the internal reference voltage at 0.6V with 1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the ds ₼ ą I × -

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The SCT2260A implements the Over-voltage Protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator

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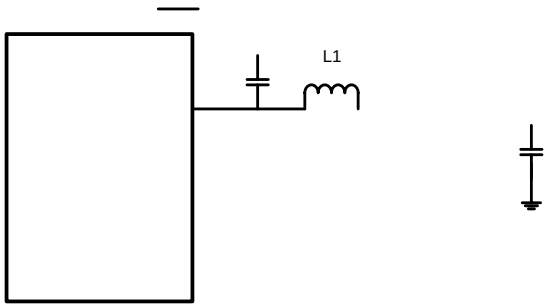

Figure 10. SCT2260A Design Example, 1V Output

Input Voltage	12V Normal 4.5V to 18V
Output Voltage	1V
Maximum Output Current	6 A
Switching Frequency	800 KHz
Output voltage ripple (peak to peak)	60mV

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For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2260A.

Use Equation 4

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The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 7 desired.

(7)

Where

Δ is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 22μF ceramic output capacitors work for most applications.

The SCT2260A features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure10. Use equation 8 to calculate the resistor divider values.

(8)

400	1.0	0.68	6.8	10.2	N/A
	3.3	2.2	45.9	10.2	100
	5.0	3.3	75.0	10.2	220
800	1.0	0.56	6.8	10.2	N/A
	3.3	1.5	45.9	10.2	100
	5.0	2.2	75.0	10.2	220
1200	1.0	0.47	6.8	10.2	N/A
	3.3	1.2	45.9	10.2	100
	5.0	1.5	75.0	10.2	220

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Unless otherwise noted, the following conditions are VIN=12V, VOUT=1V, Temperature=25C.

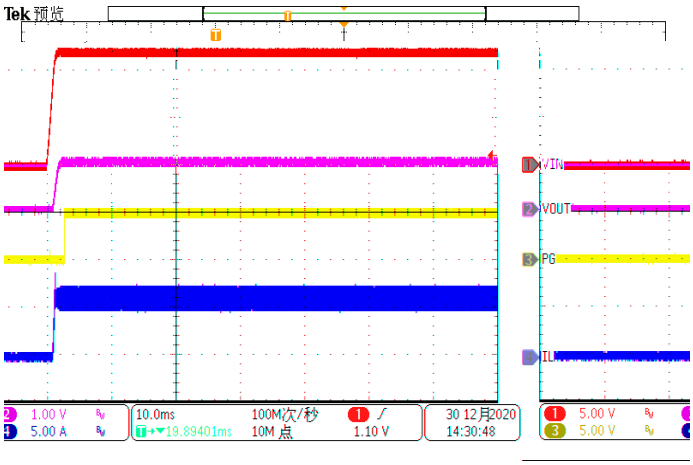

Figure 11. Power up

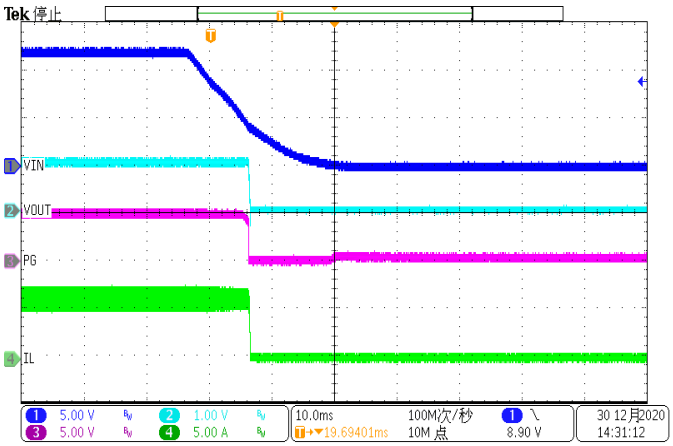

Figure 12. Power down

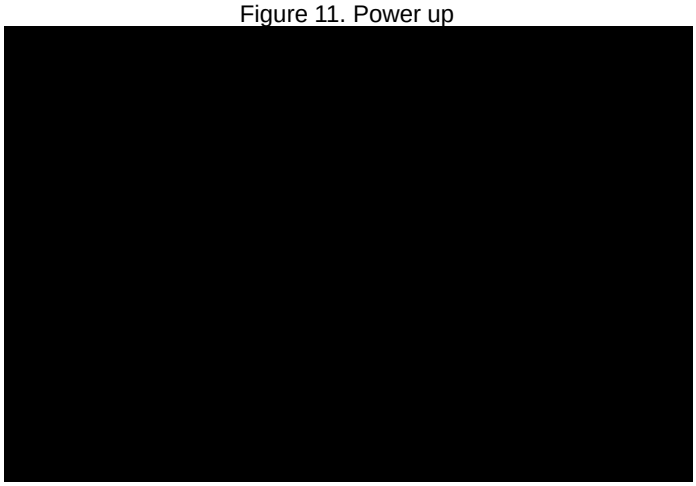

Figure 13. EN toggle (Iload=6A)

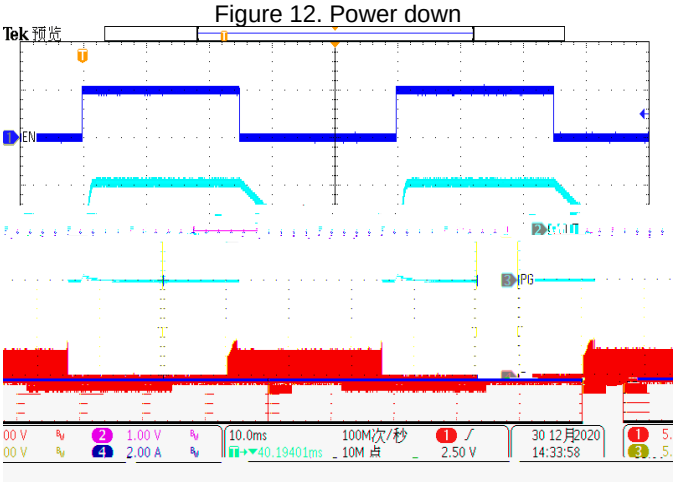

Figure 14. EN toggle (Iload=10mA)

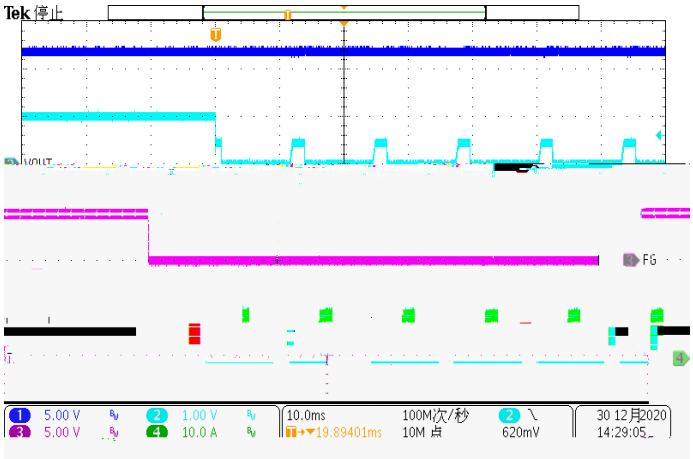

Figure 15. Over Current Protection(1A to hard short)

Figure 16. Over Current Release (hard short to 1A)

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Unless otherwise noted, the following conditions are VIN=12V, VOUT=1V, Temperature=25C.

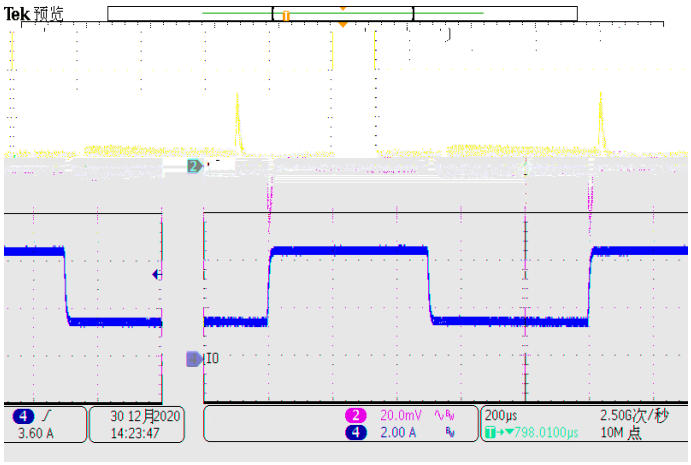

Figure 17. Load Transient (1.5A-4.5A, 1.6A/us)

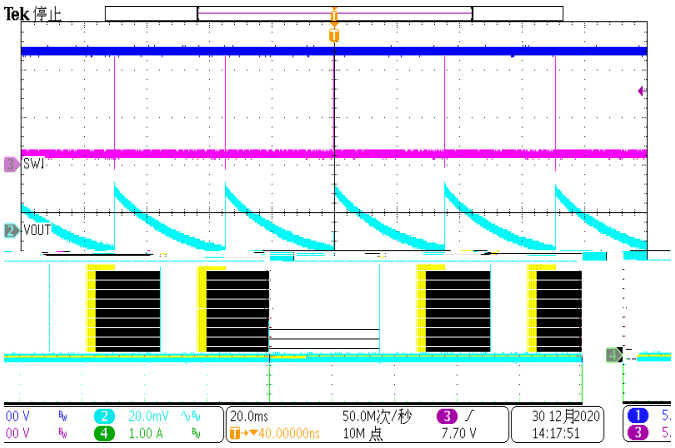

Figure 18. Output Ripple (Iload=0A, PFM)

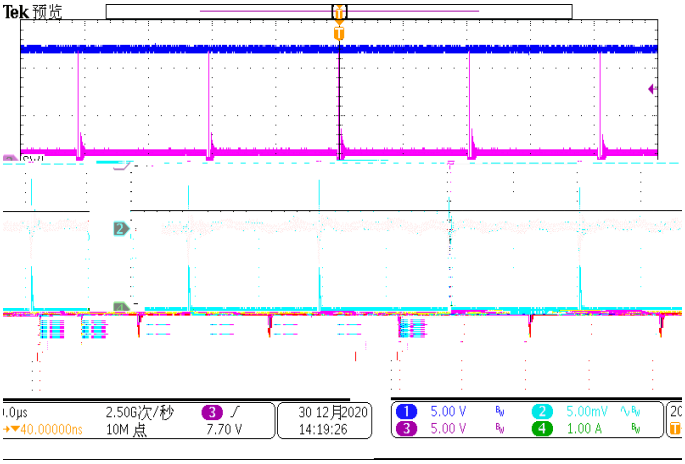

Figure 19. Output Ripple (Iload=0A, USM)

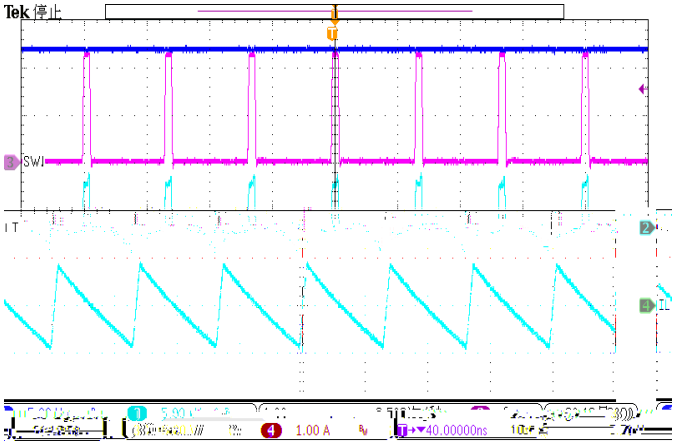

Figure 20. Output Ripple (Iload=0A, FPWM)

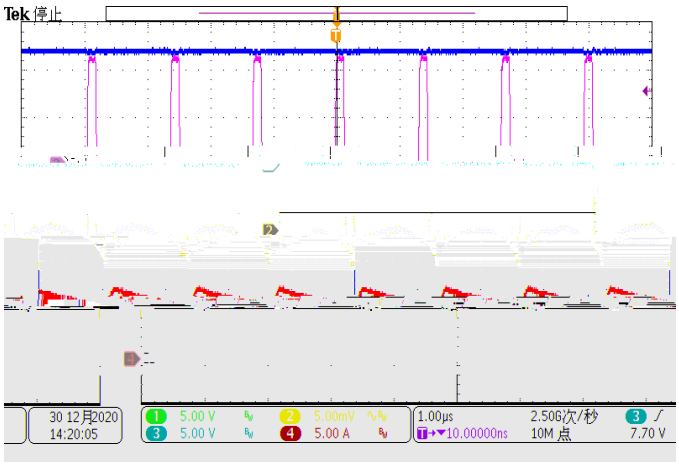

Figure 21. Output Ripple (Iload=6A)

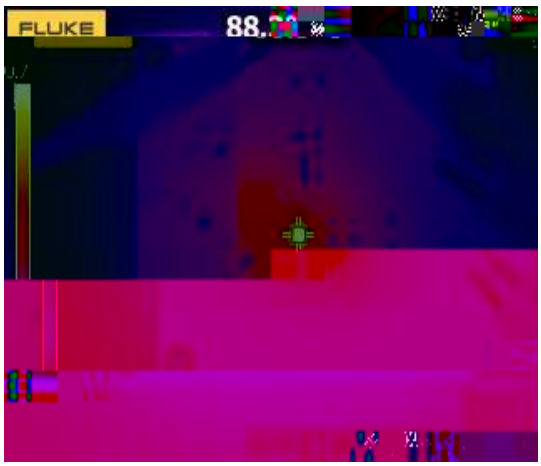

Figure 22. Thermal, 12 VIN, 1 Vout, 6A

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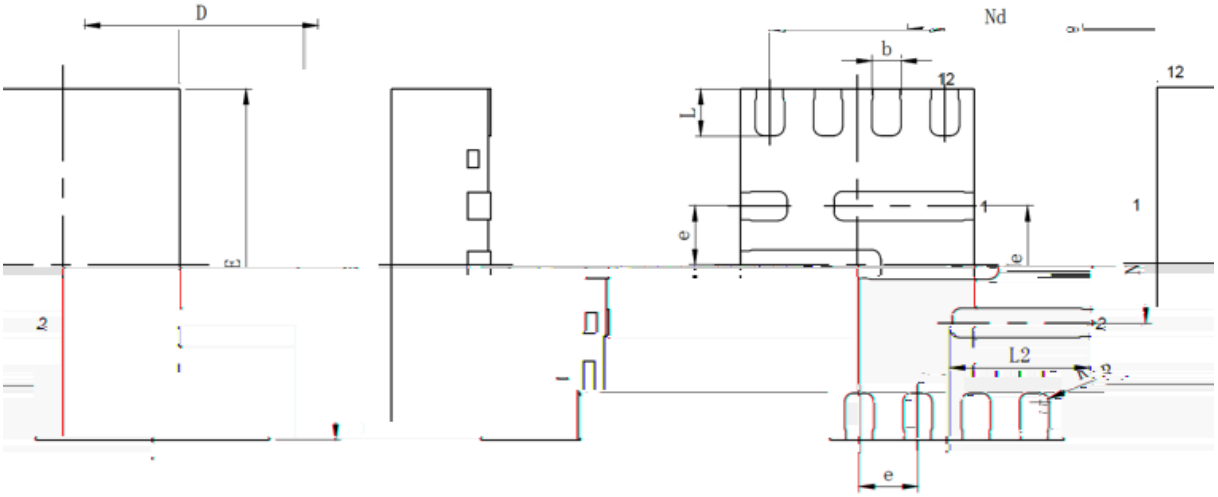

	0.80	0.85	0.90
	0	0.02	0.05
	0.20	0.25	0.30
	0.15	0.20	0.25
	1.95	2.00	2.05
	0.50BSC		
	1.50BSC		
	1.00BSC		
	2.95	3.00	3.05
	0.35	0.40	0.45
	1.15	1.20	1.25
	0.075REF		

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. Thermal pad shall be soldered on the board.
4. Dimensions of exposed pad on bottom of package do not include mold flash.
5. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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