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FSEL	4	Switching frequency selection. Connecting to ground sets clock frequency to 400KHz. Floating sets clock frequency to 800KHz. Connecting to VCC sets clock frequency to 1.2MHz.
VOUT	5	

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP

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S= 225

Overview

The SCT2250 is a 4.5V-18V input, 5A continuous output synchronous buck converter with built-in 42mΩ Rdson high-side and 17mΩ Rdson low-side power MOSFETs. It implements the Constant on-time (COT) mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is selectable, 400kHz, 800kHz and 1.2MHz, by setting different FSEL status, to optimizes either the power efficiency or the external components' sizes. The SCT2250 features an internal 1ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device features three different operation modes at light loading: Pulse Frequency Modulation (PFM) mode, Ultra-Sonic Modulation (USM) mode and Force Pulse Width Modulation (FPWM) mode. The quiescent current is typically 140uA under no load and sleep mode condition to achieve high efficiency at light load.

The SCT2250 has a default input start-up voltage of 4.25V with 300mV hysteresis. The EN function features with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN with a 100k

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zero, the low-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

Enable and Under Voltage Lockout Threshold

The SCT2250 is enabled when the VIN pin voltage rises above 4.5V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 4V or when the EN pin voltage is below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{\text{قچجج}} \text{ سي } \rho.\rho\psi \text{ z } \text{ضي}\rho \text{ طى } \frac{R\rho}{R\varsigma} \text{ ضي طي } \rho.\upsilon uA \text{ z } R\rho \qquad (1)$$

$$V_{\text{قچقق}} \text{ سي } \rho.\rho \text{ z } \text{ضي}\rho \text{ طى } \frac{R\rho}{R\varsigma} \text{ ضي طي } \upsilon.\upsilon uA \text{ z } R\rho \qquad (2)$$

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Table 1. FSEL Pin Set-up for Switching Frequency Selection

FSEL Set-up	Connect to GND	Floating	Connect to VCC
Switching Frequency	400KHz	800KHz	1200KHz

Mode Selection

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Thermal Shutdown

The SCT2250 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 150C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 125C, the device restarts with internal soft start phase.

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Typical Application

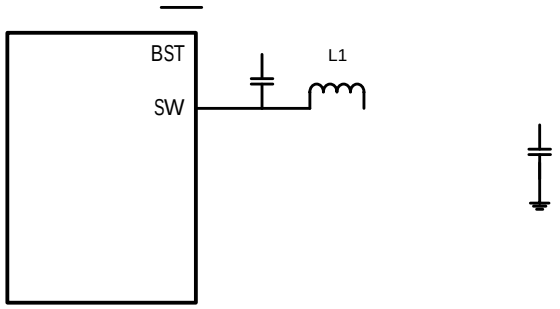

Figure 10. SCT2250 Design Example, 1.0V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 4.5V to 18V
Output Voltage	1.0V
Maximum Output Current	5 A
Switching Frequency	800 KHz
Output voltage ripple (peak to peak)	36mV

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Application Waveforms

Unless otherwise noted, the following conditions are VIN=12V, VOUT=1V, Temperature=25C.

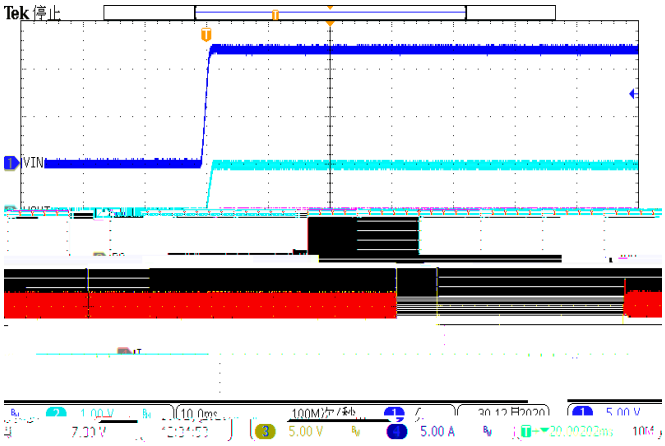

Figure 11. Power up

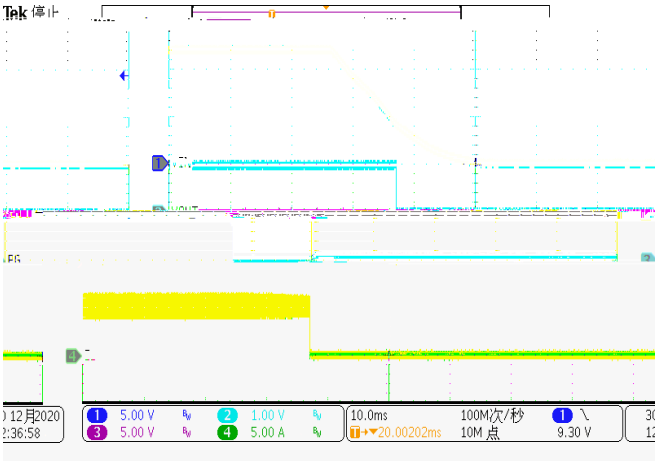

Figure 12. Power down

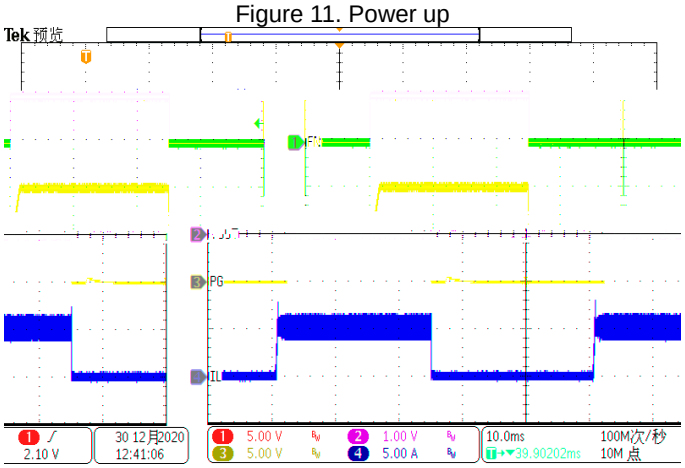

Figure 13. EN toggle (Iload=5A)

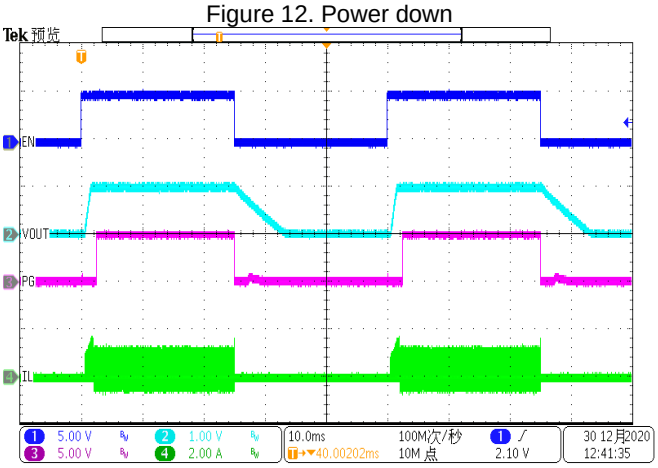

Figure 14. EN toggle (Iload=10mA)

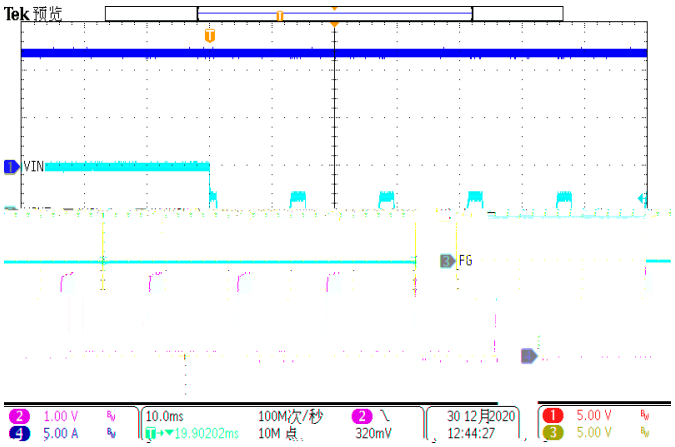

Figure 15. Over Current Protection(1A to hard short)

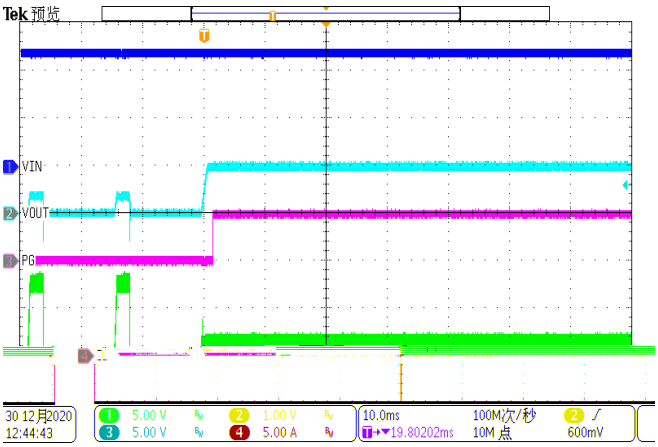

Figure 16. Over Current Release (hard short to 1A)

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Application Waveforms(Continued)

Unless otherwise noted, the following conditions are VIN=12V, VOUT=1V, Temperature=25C.

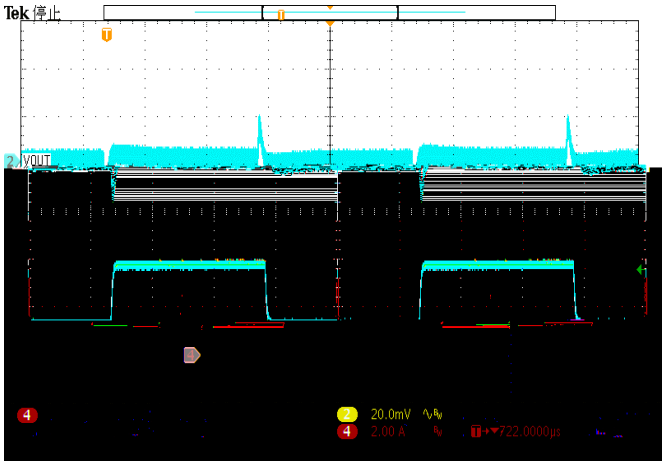

Figure 17. Load Transient (1.25A-3.75A, 1.6A/us)

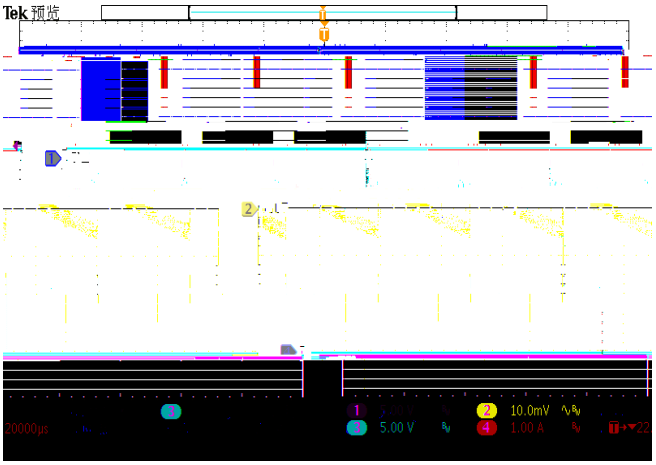

Figure 18. Output Ripple (Iload=0A, PFM)

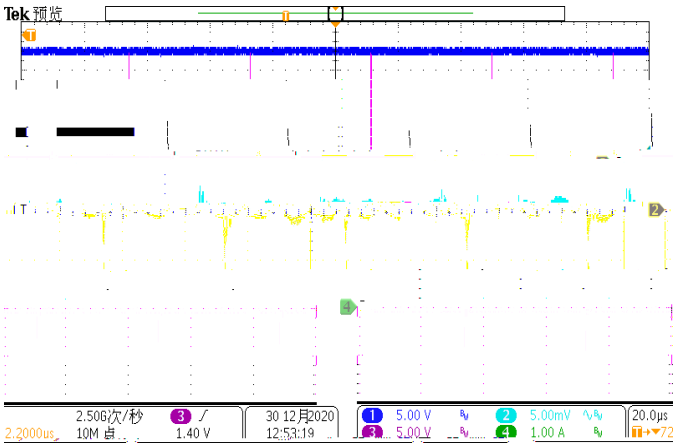

Figure 19. Output Ripple (Iload=0A, USM)

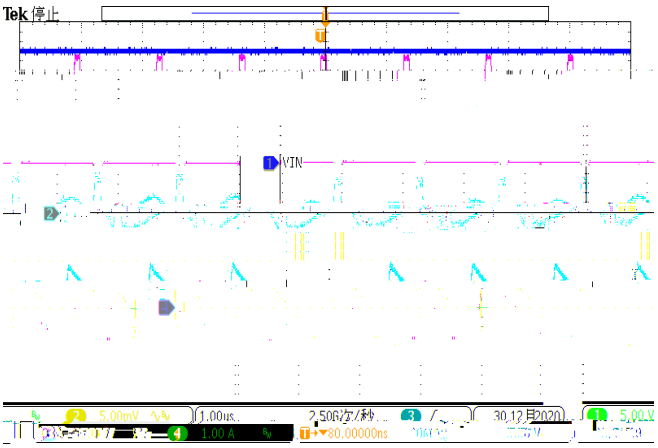

Figure 20. Output Ripple (Iload=0A, FPWM)

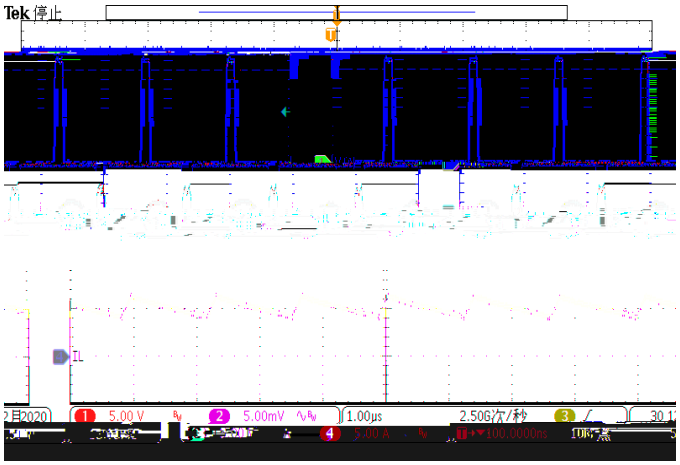

Figure 21. Output Ripple (Iload=5A)

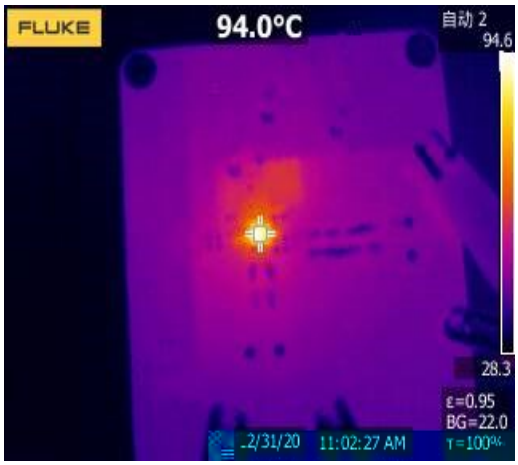

Figure 22. Thermal, 12 VIN, 1 Vout, 5A

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Layout Guideline

Proper PCB layout is a critical for SCT2250's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
2. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
3. .

4. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
5. UVLO adjust and loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
6. Route BST resistor and capacitor with a minimized length between the BST PIN and SW PIN.

Figure 23. PCB Layout Example

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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90

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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	328	329	330
B	11.80	12.80	13.80
C	99	100	101
D	13.00	13.30	13.60
t	1.70	2.00	

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