19V Vin Quad Channel Power Management IC for Automotive Applications

FEATURES

Qualified for Automotive Applications
AEC-

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

THERMAL INFORMATION (continued)

PARAMETER	THERMAL METRIC	QFN- 0 T1 [(.1 /C.1 s 0 549 9 /)7

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~150°C, typical values are tested under 25°C

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PEAK_TU						
I						

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

TYPICAL CHARACTERISTICS

V_{IN}=10V, T_A=-40°C~125°C, unless otherwise noted.

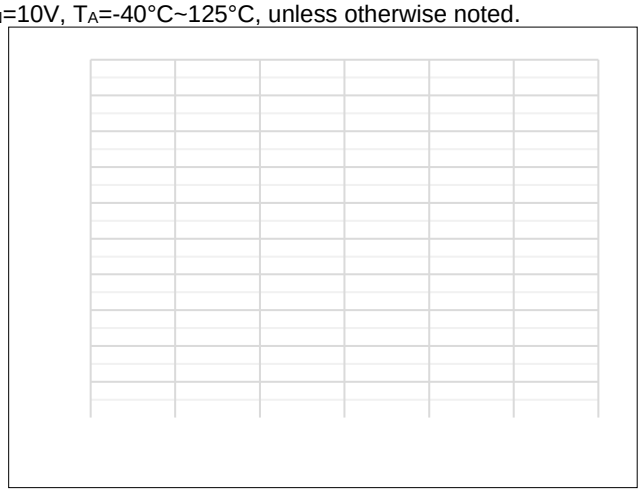


Figure 1. Buck1 Efficiency vs Load Current, V_{OUT1}=3.2V

Figure 2. Buck1 Efficiency vs Load Current, V_{OUT1}=3.0V

Figure 3. Buck2 Efficiency vs. Load Current, V_{OUT2}=1.8V

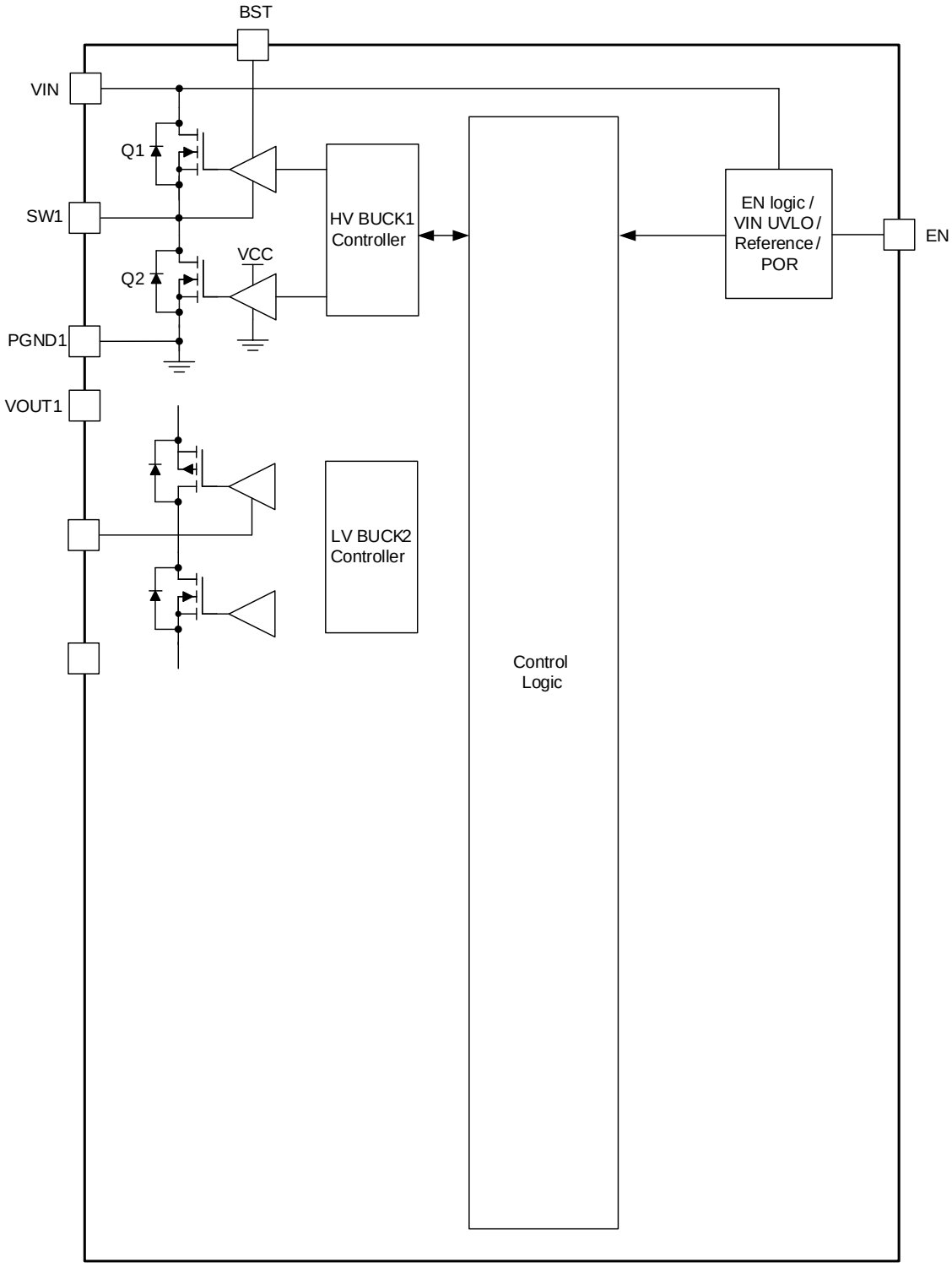
Figure 4. Buck3 Efficiency vs. Load Current, V_{OUT3}=1.2V

Figure 5. Buck3 Efficiency vs. Load Current, V_{OUT3}=1.5V

Figure 6. Buck1 Peak Current Limit vs. Temperature

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

FUNCTIONAL BLOCK DIAGRAM



 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

Under Voltage Protection

If an output falls below the under voltage protection threshold, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting. When entry hiccup, the output discharge will operate during the hiccup time.

Over Current Protection (OCP)

For the three bucks and LDO, the SCT61240Q provides both peak and valley current limit designed to limit the peak/valley inductor current to ensure that the switching currents remain within the device capabilities during overload conditions or during an output short circuit.

When the HS-FET turns on, the chip monitors the increased IL through the relevant operating main power switch. Once the peak IL exceeds the peak current limit threshold, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease IL. The HS-FET does not turn on again until IL falls below the valley current limit threshold.

Power Good

The PG pin is a push-pull output. It goes to logic high when the device is powered on, and all outputs are within the power good range, and no faults reported. The high output level can be programmed to either 3.3V or 1.8V.

PG will assert low when any of below events occur:

Buck1's output is out of power good range or VOUT OV/UV range

Buck2's output is out of power good range or VOUT OV/UV range

Buck3's output is out of power good range or VOUT OV/UV range

LDO's output is out of power good range or VOUT OV/UV range

Junction temperature is over Thermal Shutdown point

VIN is higher than VIN OVP threshold

Hiccup or Latch off Protection

When below faults are detected, the SCT61240Q will enter hiccup or latch off mode (programmable option). When select hiccup mode and entry hiccup, all the channels shut off for 3.6ms, and then the normal power up sequence will start again according to the SEQ and RSET setting. When select latch off mode and entry latch off, all the channels shut off and not restart unless VIN/EN power on reset (POR).

The faults that make the device entry hiccup/latch off protection:

Buck1's output is out of VOUT OV/UV range

Buck2's output is out of VOUT OV/UV range

Buck3's output is out of VOUT OV/UV range

LDO's output is out of VOUT OV/UV range

Junction temperature is over Thermal Shutdown point

VIN is higher than VIN OVP threshold

Output Discharge

In order to discharge the energy of output capacitor during power off sequence, all channels have active discharge path from their output to ground. The discharge path is turn-on when channel is disabled.

Internal Soft-Start

The soft start function is implemented to prevent the PMIC output voltage from overshooting during start-up. When

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

APPLICATION INFORMATION

Typical Application

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of R_1 and R_2 resistors.

$$8_{å Ü æ ø} l1 + \frac{4_5}{4_6} p Û8_{¾ ç å Ü æ ø} \quad (1)$$

$$8_{Ù Ô ß ß} l1 + \frac{4_5}{4_6} p Û8_{¾ Ç Ù Ô ß ß} \quad (2)$$

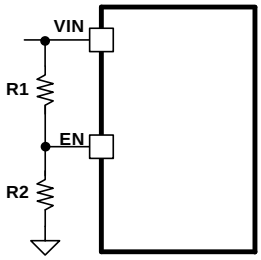


Figure 14. System UVLO by enable divide

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

V_{ENrise} is rising threshold of EN UVLO

V_{ENfall} is falling threshold of EN UVLO

Inductor Selection

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

$V_{IN(max)}$ is the maximum input voltage

$I_{OUT(max)}$ is the maximum DC load current

LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{6}$$

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

-4

Application Waveforms

Vin=10V, RSET=SEQ=8kq\, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted-4V , -

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms (continued)

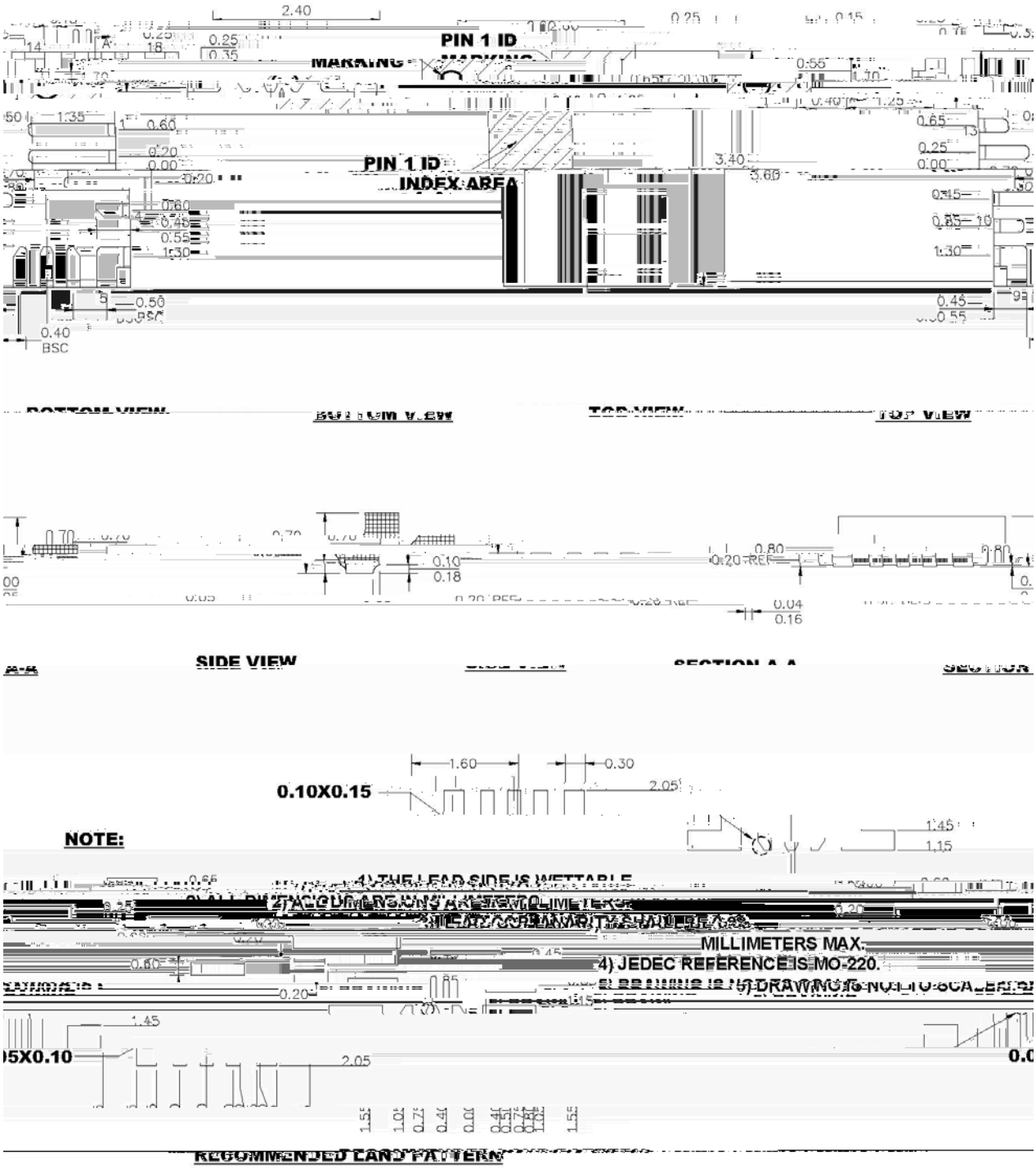
Vin=10V, RSET=SEQ=8kq\, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

Figure 21. Buck2 Over Current Protection

(0.6A to hatehon . B

 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved

PACKAGE INFORMATION



 © 2024 Silicon Content Technology Co., Ltd. All Rights Reserved