NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

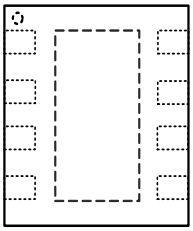
Revision 1.1: Update the Figure 8 and Figure 26 and thermal performance on page 20.

Revision 1.2: Add MSL level in device order information. Update tape and reel information.

Revision 1.3: Update the package information.

Revision 1.4: Update the package information and the soft-start time.

2UGHUDEOHQXPEHU	2XWSXW 9ROWDJH	3DFNDJH	3DFNDJH 0DUNLQJ	3,16	06/	7UDQVSRUW 0HGLXP 4XDQWLW\
SCT71010A00QDTBR	Adjust	DFN3x3-8L	0A00Q	8	1	Tape & Reel, 5000



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DFN3x3-8L Package

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$V_{IN}=V_{e(OUT)}+1V$, $C_{OUT}=10uF$

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6 < 0 % 2 /	3 $ 5 $ 0 (7 (5	7 (6 7 & 2 1 ' , 7 , 2 1	0 , 1	7 < 3	0 $;	8 1 , 7
I_{EN_0V}	Enable pin current	EN=0			0.2	εA
$I_{EN_3.3V}$	Enable pin current	EN=3.3V		0.01	0.2	

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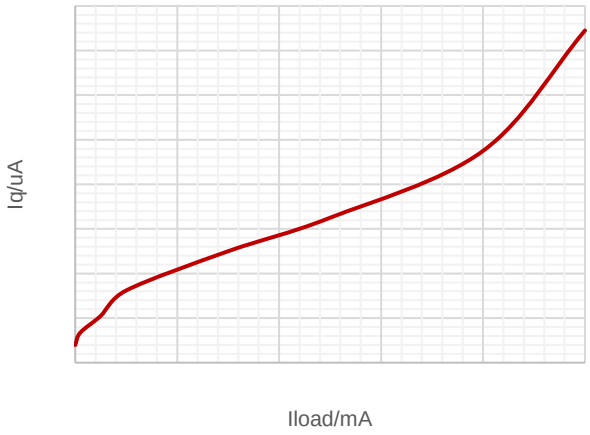


Figure 1. Quiescent Current vs Output Current

Figure 2. Quiescent Current vs Input Voltage, No load

Figure 3. Quiescent Current vs Ambient Temperature

Figure 4. Dropout Voltage vs Output Current

Figure 5. Output Voltage vs Ambient Temperature at VOUT=1.8V

Figure 6. Output Voltage vs Input Voltage

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Figure 13. PSRR vs Frequency
VIN=4.3V, Cf=33pF,COUT=10uF,IOUT=10mA

Figure 14. PSRR vs Frequency
VIN=3.3V,VOUT=1.2V,Cf=33pF,COUT=10uF

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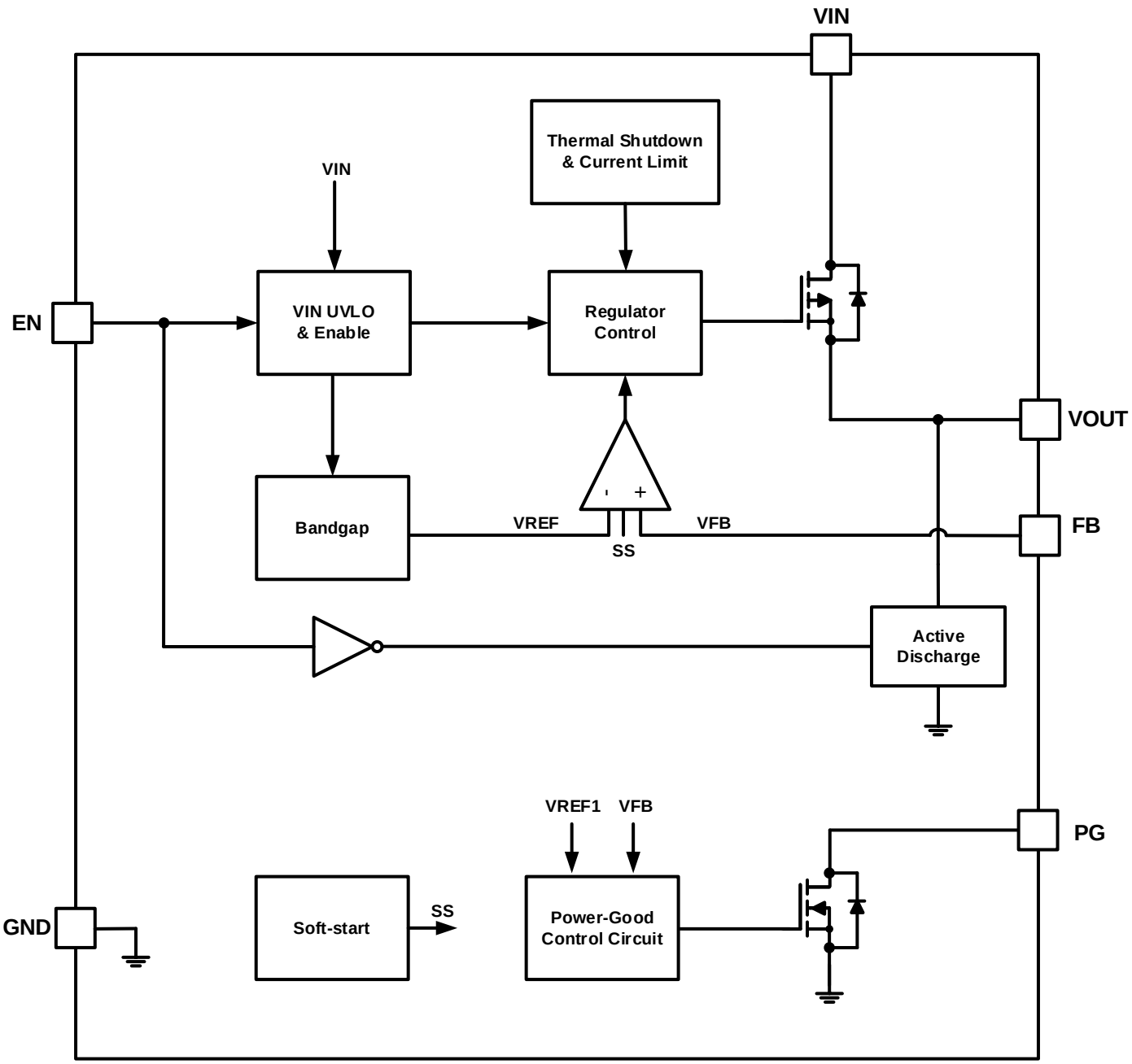


Figure 15. Functional Block Diagram of Adjust Output Version

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The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN}–V_{OUT})Ï I_{OC}]. When the output is shorted and the output voltage is less than $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN}–V_{OUT})Ï I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

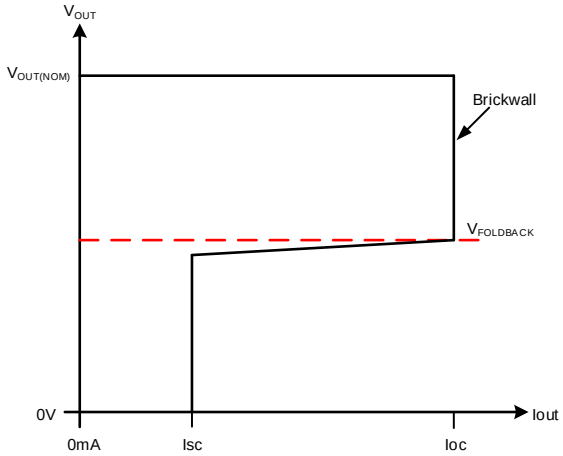


Figure 16. Current Limit with Foldback Feature

, Q W H 6 R Q 6 W D U W

The SCT71010A00Q product integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 2.4ms. If the EN pin is pulled below 0.66V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

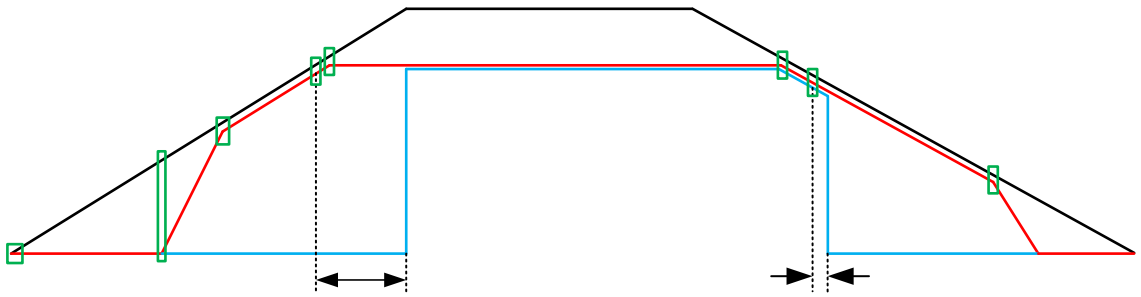


Figure 20. Startup and Shutdown Example —SCT71010Q Series

7KHUPDO 6KXWGRZQ

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

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Figure 24. SCT71010A00Q Feed Forward Capacitors recommend(R2=100kq ,VOUT=1.8V)

Figure 25. SCT71010A00Q Feed Forward Capacitors recommend(R2=10kq ,VOUT=1.8V)

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3RZHU 'LVVLSDWLRQ DQG 3DFNDJH 7KHUPDO 3HUIRUPDQFH

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3. Because $I_{GND} \ll I_{OUT}$, the term $V_{IN} \times I_{GND}$ in Equation 3 could be ignored.

(3)

The junction temperature can be estimated using Equation 4. $R_{\theta JA_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J.

(4)

$R_{\theta JA_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71010A00Q product, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the R_{JA_EVM} of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM: 4-layer,1oz Cu (inner 0.5oz Cu), 50mm x 30mm size.

7KHUPDO 3DUDPHWHUV RI 3DFNDJHV %DVHG RQ (90 7HVW

3DFNDJH	0D[$OORZDEOH 3 1RW 7UDFNHG 6JHQ87 9	0D[$OORZDEOH 7-”	5-$B(90 :
DFN3X3-8L	2.73	1.88	53.09

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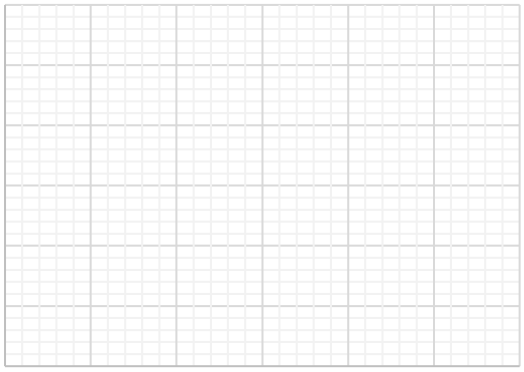


Figure 26. Maximum Output Current vs Input Voltage, VOUT=1.8V of DFN3X3-8L ,$T_J \le$ TSD_R

Figure 27. Maximum Output Current vs Input Voltage, DFN3X3-8L,TJ ≤ 125

Figure 28. Maximum Allowed Power Dissipation vs Ambient Temperature, DFN3X3-8L,TJ ≤ 125

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$SSOLFDWLRQ :DYHIRUPV &RQWLQXHG

Vin=Vout +1V, unless otherwise noted

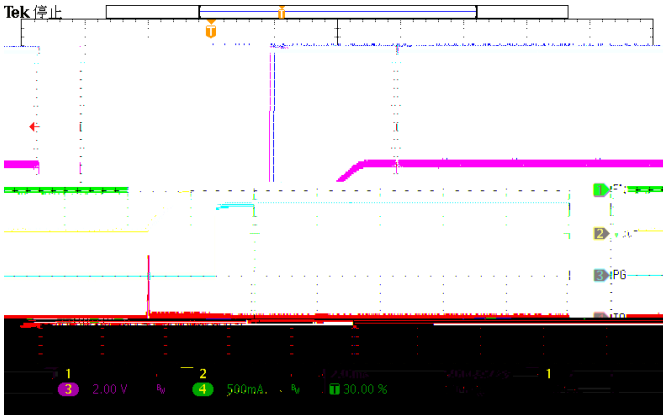


Figure 35. Enable (Iload=10mA)

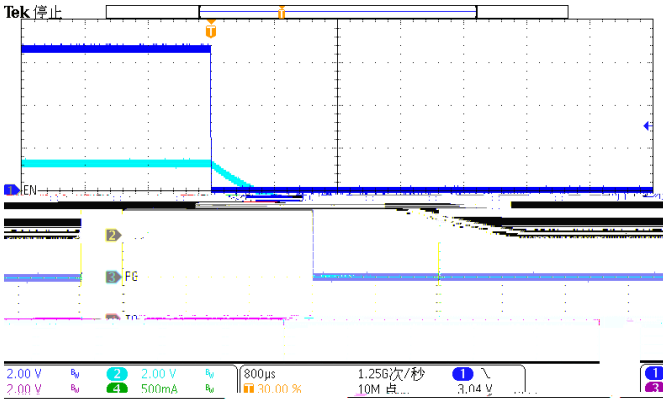


Figure 36. Disable (Iload=10mA)

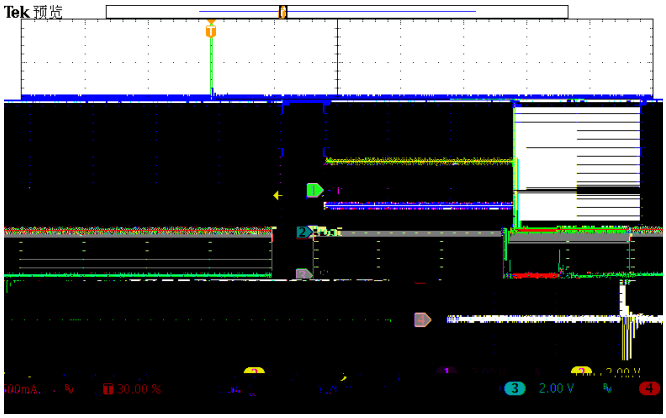


Figure 37. Enter Short Circuit Protection

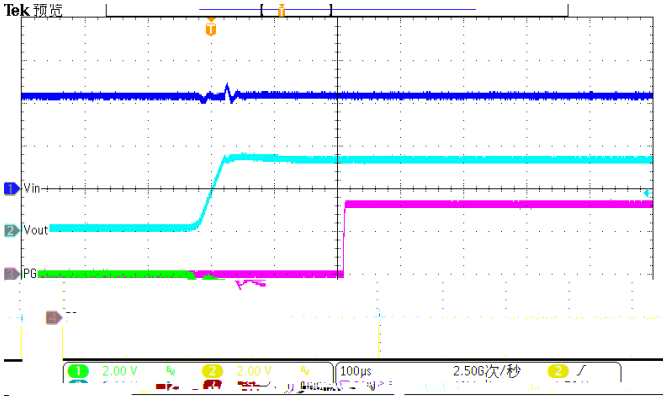


Figure 38. Exit Short Circuit Protection

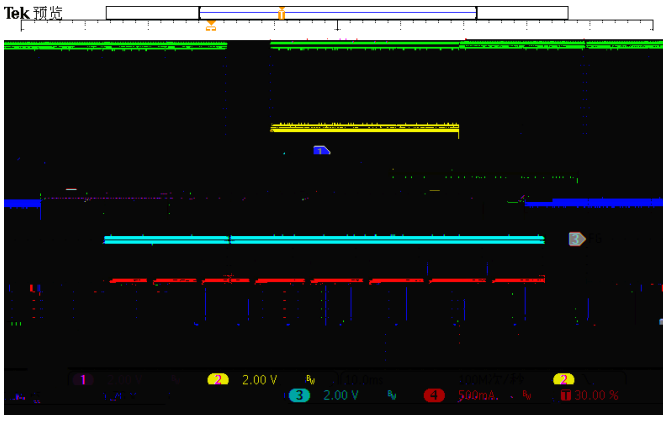


Figure 39. Enter Over Temperature Protection(Vin=5.5V)

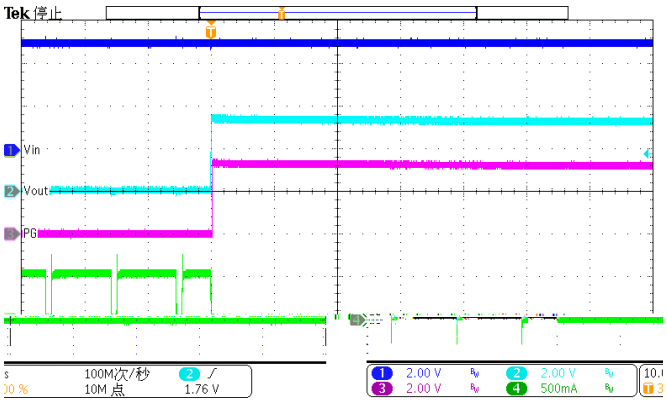


Figure 40. Exit Over Temperature Protection(Vin=5.5V)

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/D\RXW *XLGHOLQH

Proper PCB layout is a critical for SCT71010Qôs stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1εF bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize IĭR drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT recommends adding a 10uF low ESR capacitor parallel connection with the large electrolytic capacitor.

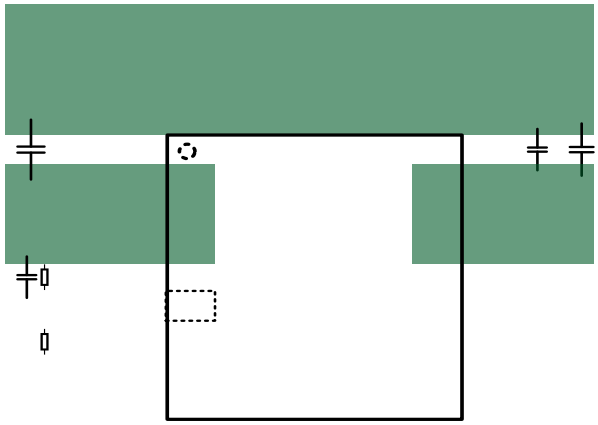


Figure 41. PCB Layout Example

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DFN3x3-8L xM Ae · ɹ j ɔ ʊ t

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