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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

Revision 1.1: Update DEVICE ORDER INFORMATION.

Revision 1.2: Update V_{FB} Max limit to 0.82V in EC, add MSL.

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V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		4.5	40	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	4.3		V
	Hysteresis		440		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V	1	5	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V	90		

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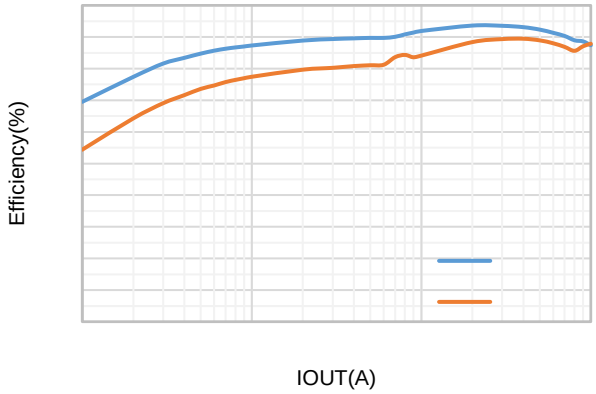

Figure 1. Efficiency vs Load Current, Vout=5V

Figure 2. Efficiency vs Load Current, Vout=12V

Figure 3. Load Regulation, Vout=5V, Vin=24V

Figure 4. Line Regulation, Vout=5V, Io=0.5A

Figure 5. Reference VS Temperature

Figure 6. HS Current Limit VS Temperature

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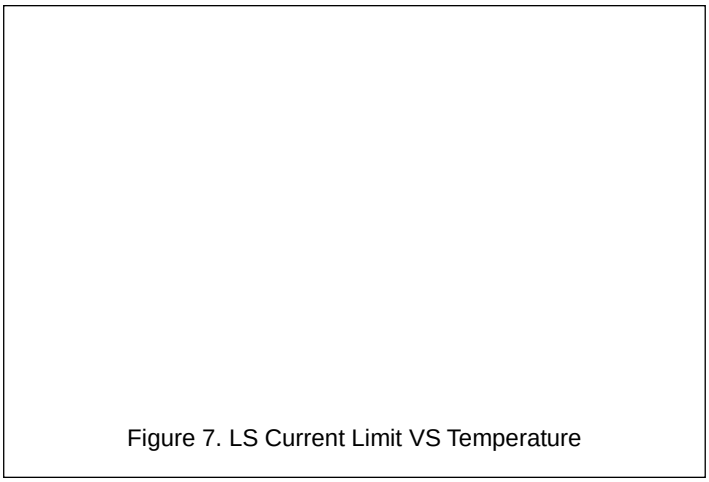

Figure 7. LS Current Limit VS Temperature

Figure 8. Quiescent Current vs Temperature Vin=12V

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PEAK HIGH EFFICIENCY

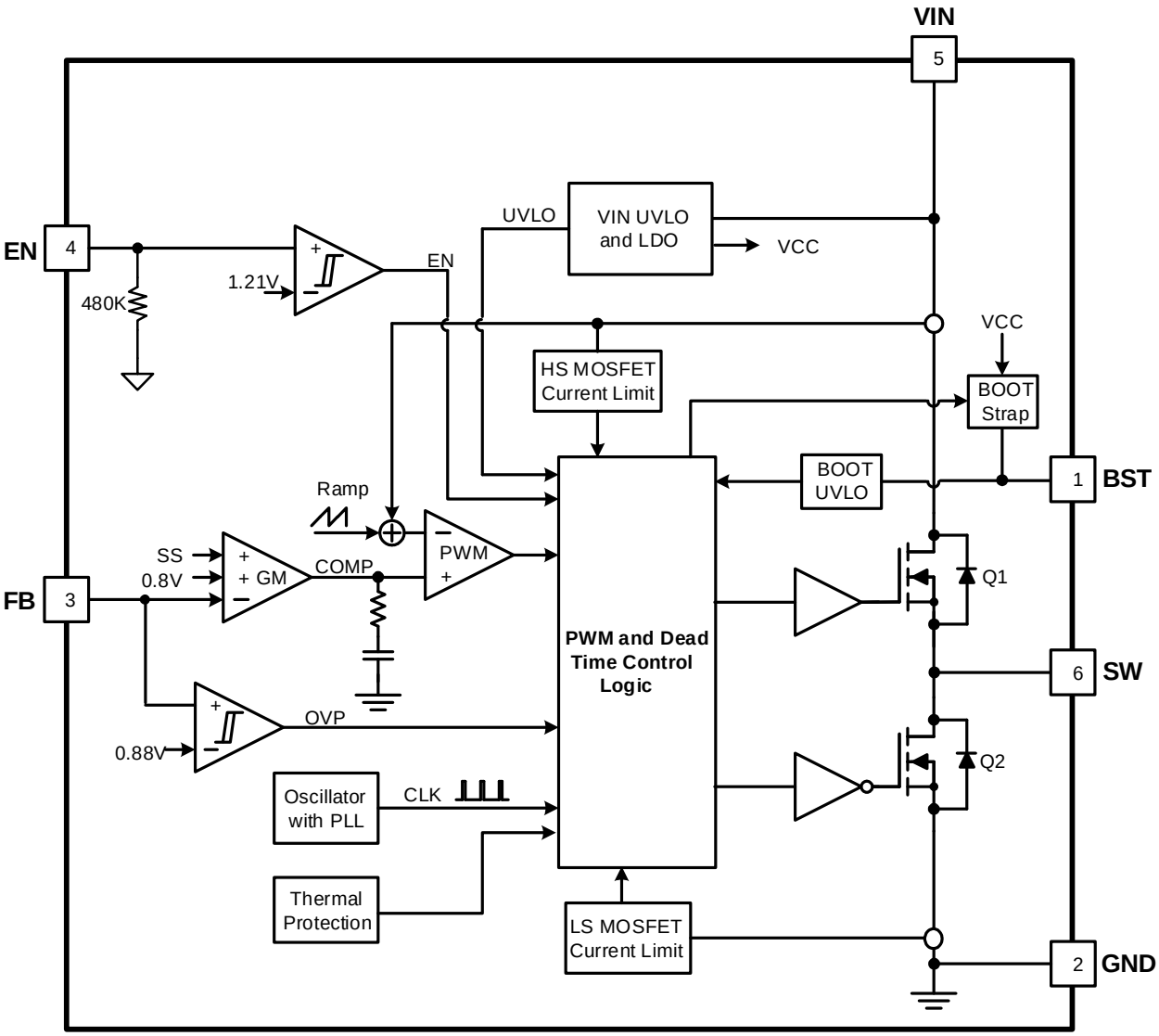

Figure 13. Functional Block Diagram

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The SCT2411 device is 4.5V-40V input, 1A output, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 1.2MHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 1ms soft-start simplify the SCT2411 footprints and minimize the off-chip component counts. Meanwhile, it reduces the external passive components size as well.

The quiescent current of SCT2411 is 90uA typical under no-load and without switching condition. When disabling the device, the supply shut down current is only 1μA. The SCT2411 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition.

The SCT2411 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2411 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 160mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss.

The SCT2411

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and the device starts soft-start phase. The SCT2411 has the built in 1ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/falling).

An internal 480k pull down resistor make EN pin floating shut down the SCT2411

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The SCT2411 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient.

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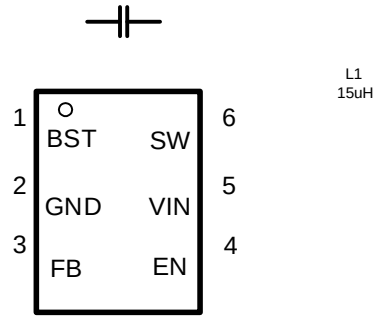

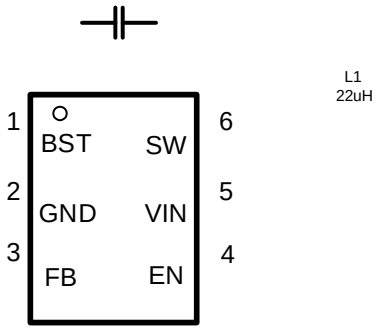

Design Parameters	Example Value
Input Voltage	24V
Output Current	1A
Switching Frequency	1.2MHz
Start Input Voltage (rising VIN)	5.5V
Stop Input Voltage (falling VIN)	5V

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The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 20KΩ. Use Equation 4 to calculate R1.

(4)

where:

V_{REF} is the feedback reference voltage, typical 0.8V

Table 1. R_1, R_2Value for Common Output Voltage (Room Temperature)

1.8 V	24.9 KΩ	20 KΩ
2.5 V	42.2 KΩ	20 KΩ
3.3 V	62 KΩ	20 KΩ
5 V	105 KΩ	20 KΩ

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For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

(13)

For this example, a 4.7μF, X7R ceramic capacitors rated of 50 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

(14)

Where

Δ is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

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V_{IN}=24V, V_{OUT}=5V, unless otherwise noted

Figure 18. Power up (I_{LOAD}

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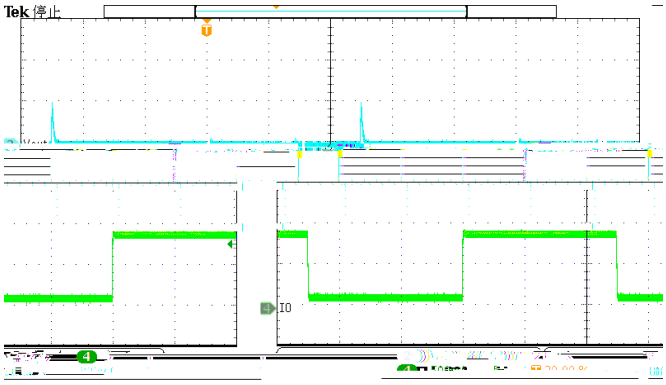

Figure 24. Load Transient (0.1A-0.9A, 1.6A/us)

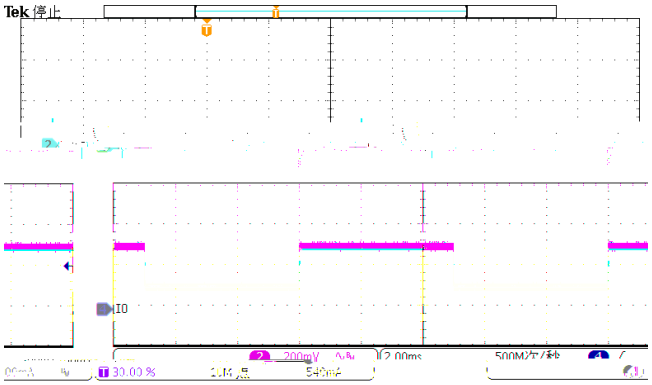

Figure 25. Load Transient (0.25A-0.75A, 1.6A/us)

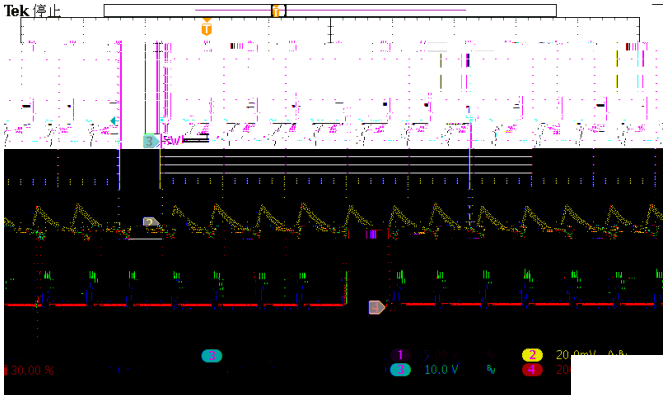

Figure 26. Output Ripple (I_{LOAD}=10mA)

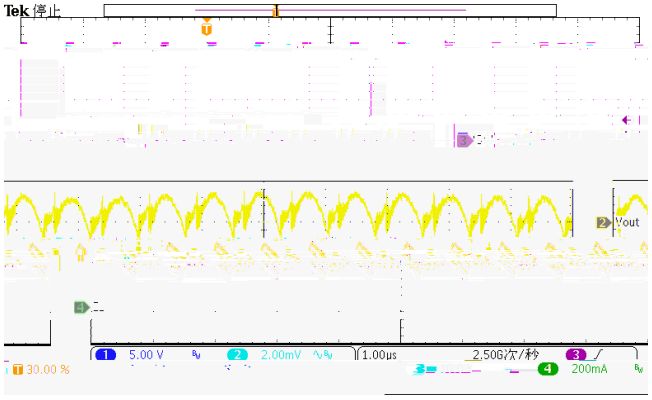

Figure 27. Output Ripple (I_{LOAD}=0.2A)

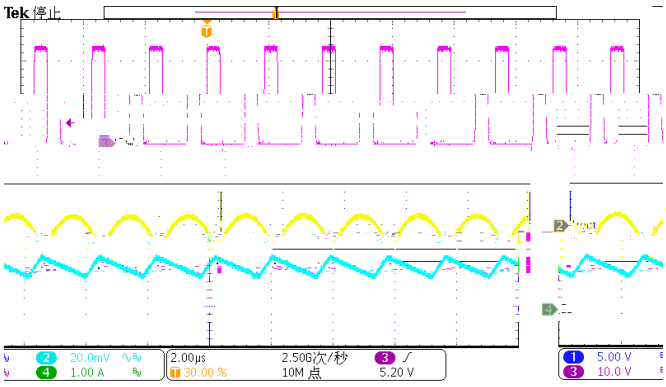

Figure 28. Output Ripple (I_{LOAD}=1A)

Figure 29. Thermal, 24V_{IN}, 5V_{OUT}, 0.8A

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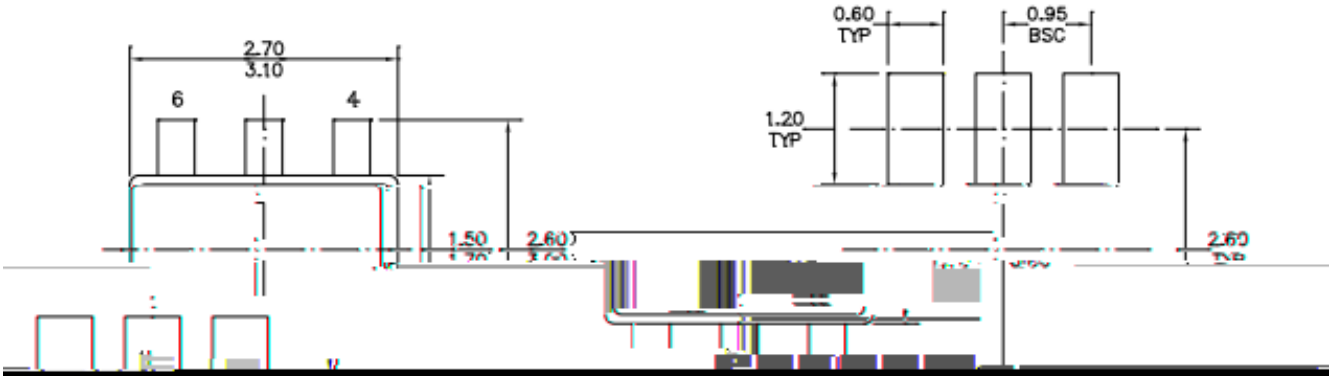

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