ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL

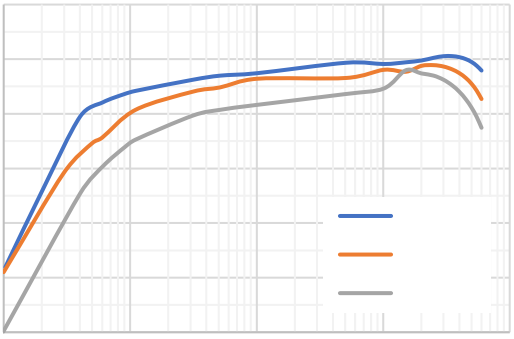
DESCRIPTION	MIN	MAX	UNIT

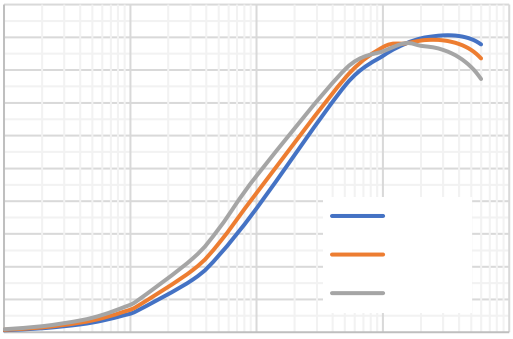


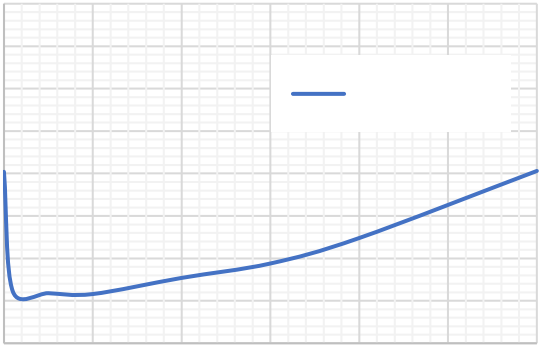
Top View: SOT563-6

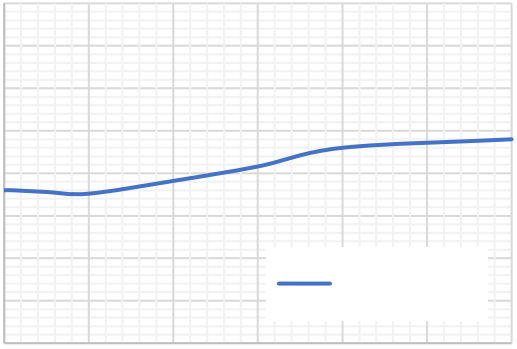
PARAMETER	DEFINITION	MIN	MAX	UNIT

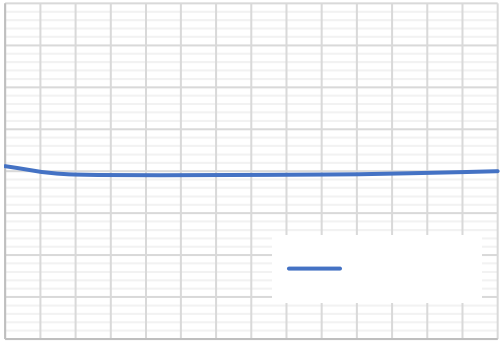
SYMBOL	PARAMETER	TEST CONDITION	MIN

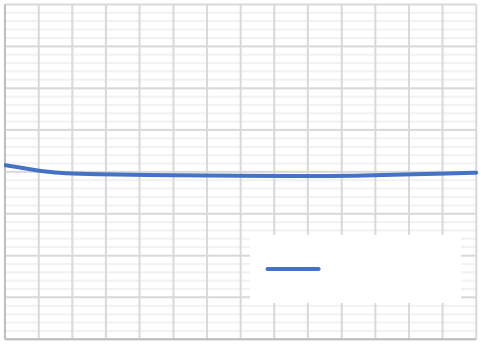












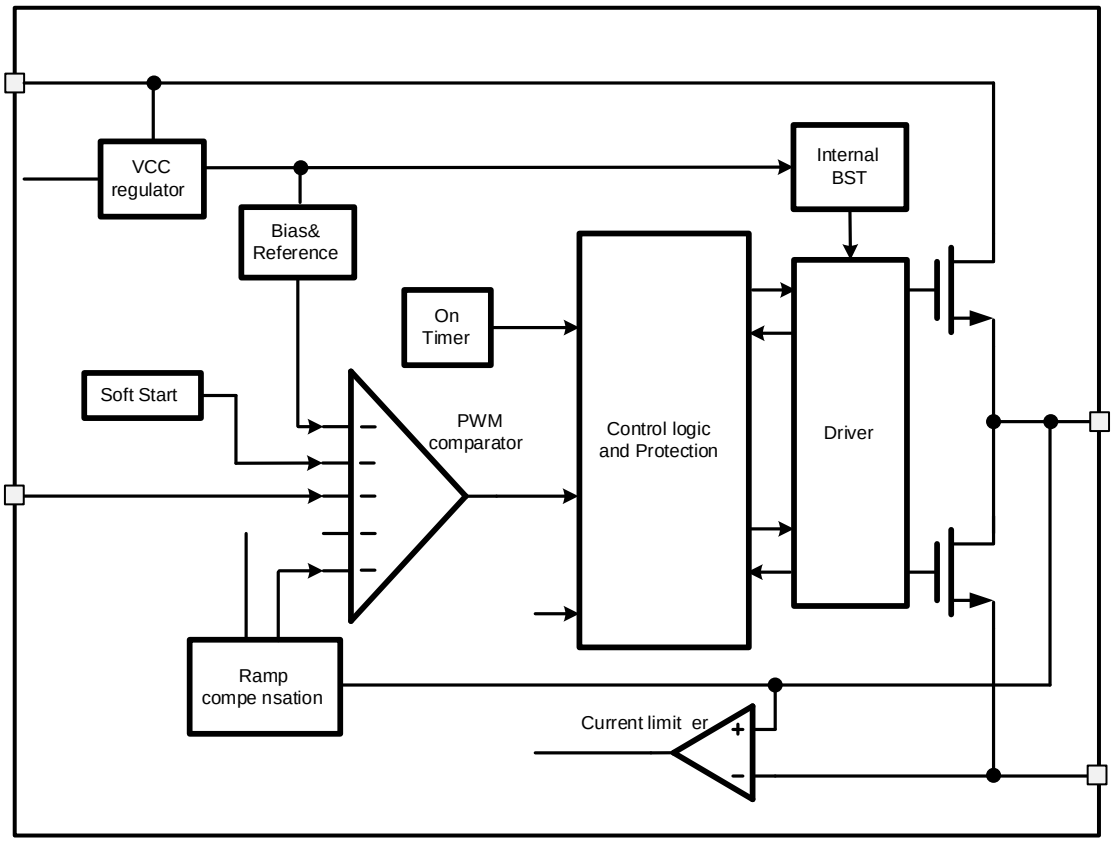


Figure 13. Functional Block Diagram

Overview

Forced Continuous Conduction Mode (FCCM)

Enable and Start Up

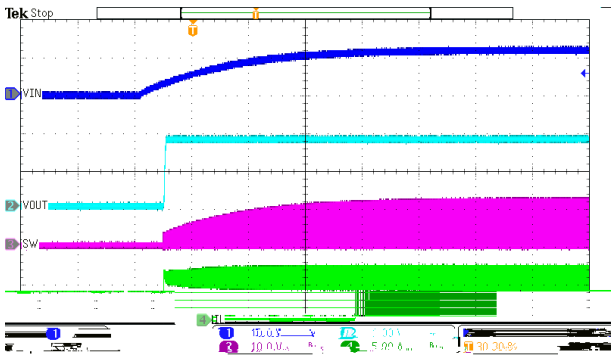
Output Voltage

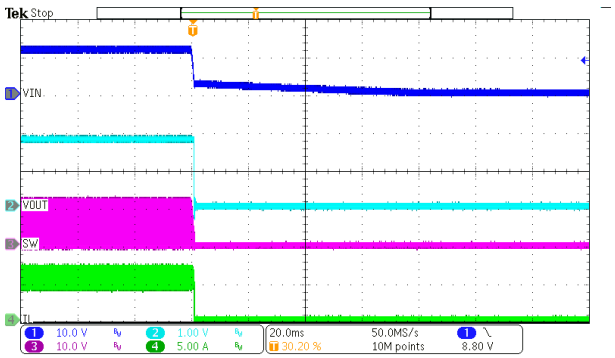
Under Voltage Lockout UVLO

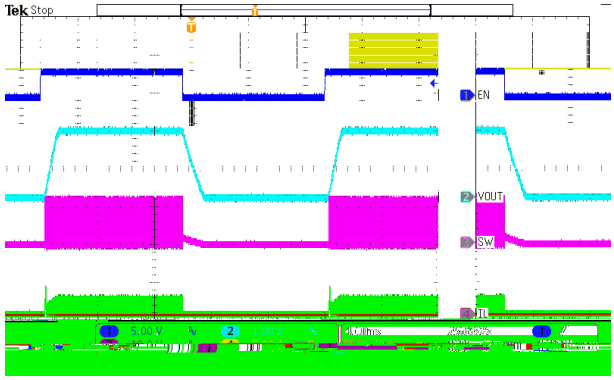
Over Current Protection (OCP) and Hiccup Mode

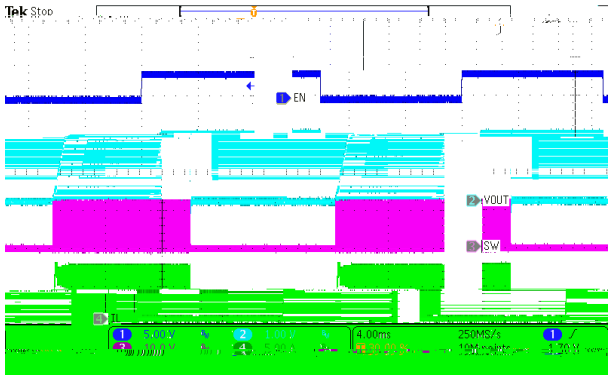
Thermal Shutdown

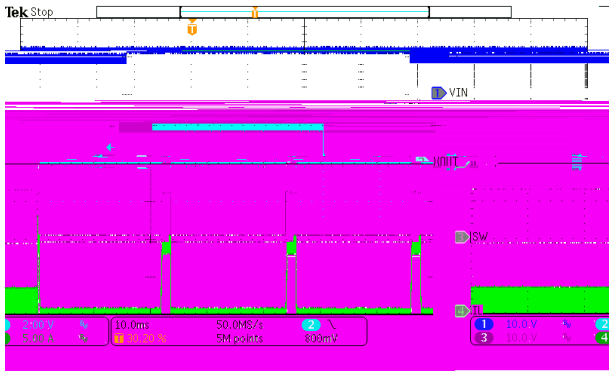
Application Waveforms

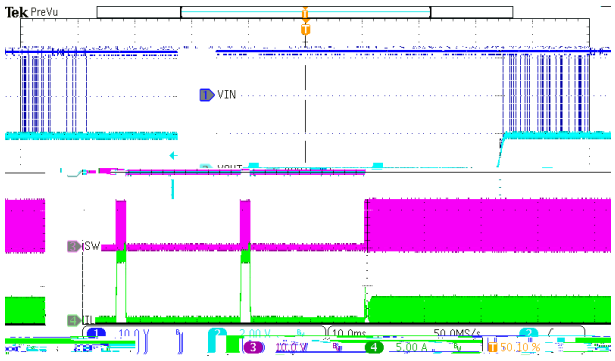












Application Waveforms

Output Voltage

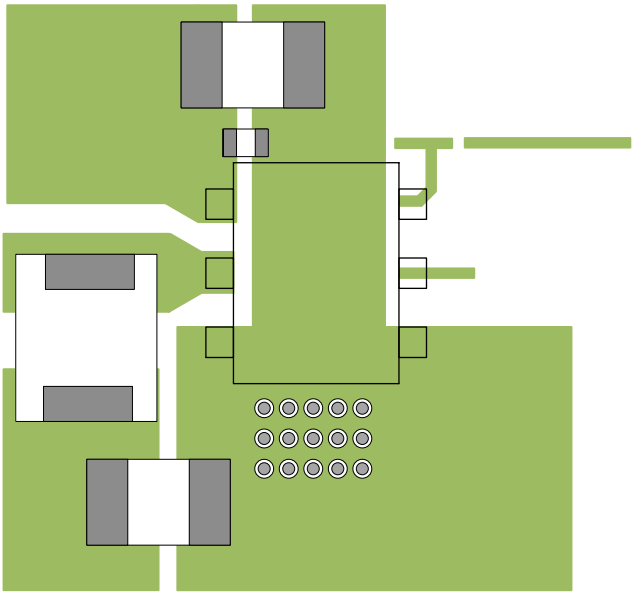
V_{OUT}	R_1	R_2

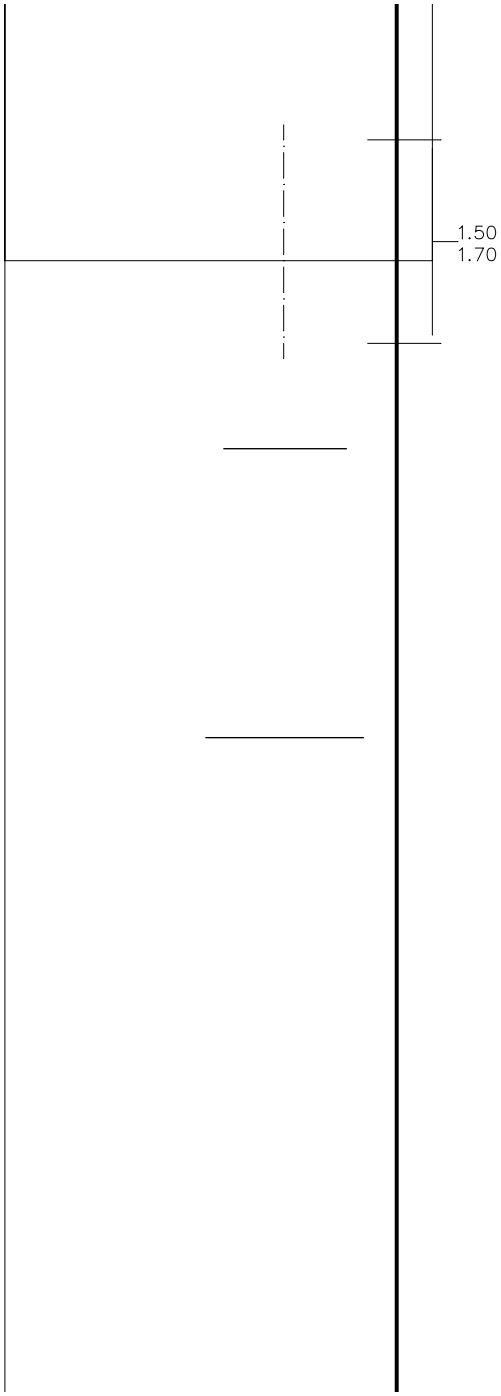
Inductor Selection

Layout Guideline

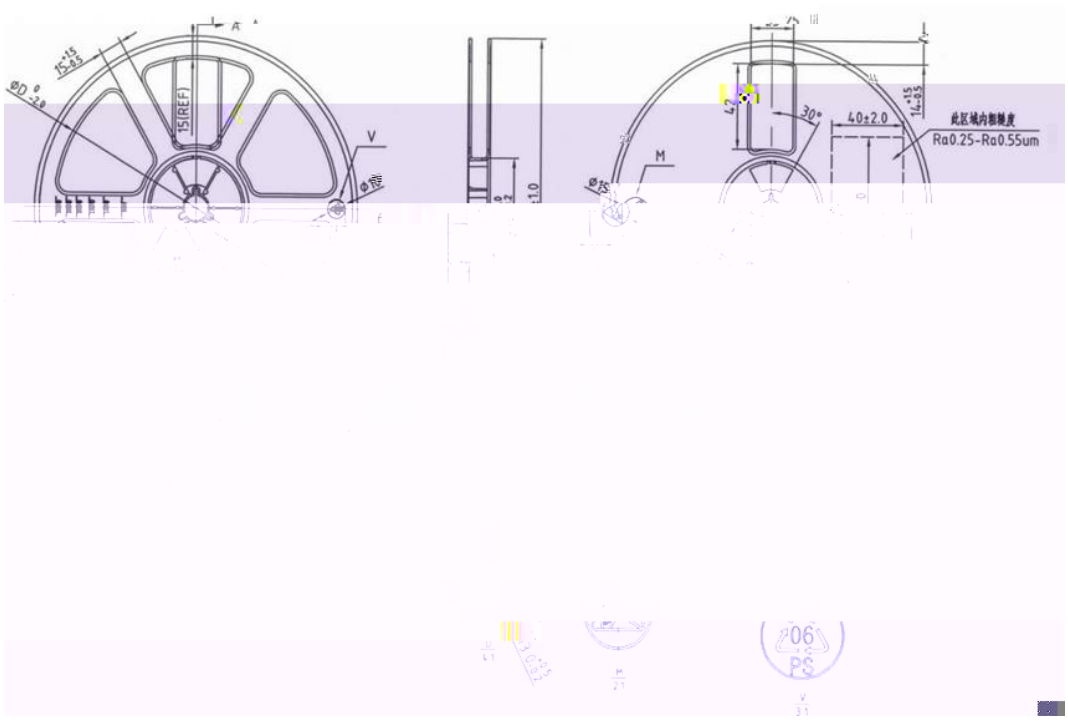
The bottom layer is a large ground plane connected to the ground plane on top layer by vias.

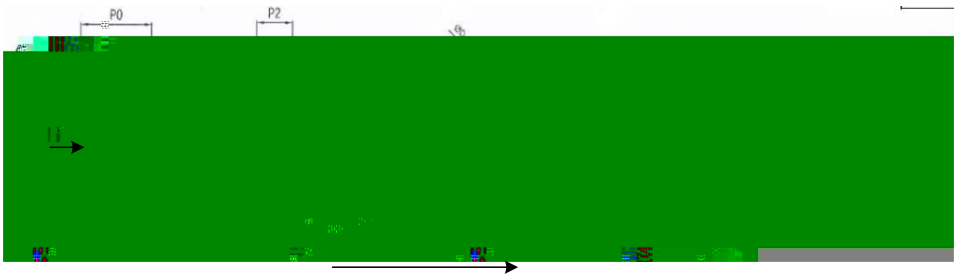
soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss through the vias is of concern, plugging or tenting can be used to achieve a repeatable process.





1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-293, VARIATION UAAD.
6) DRAWING IS NOT TO SCALE.





☆W	8.00 +0.30 -0.30	E	1.75±0.10
☆B	4.00±0.10	F	3.50±0.05
☆A0	1.80±0.05	P2	2.00±0.05
☆B0	4.32±0.05	D	1.5 +0.10 0
☆K0	0.75±0.10	D1	0.50±0.05
t	0.30±0.02	P0	4.00±0.10
10P0	40.0±0.20	θ	5° MAX

